PARAMAX
Une compagnie Unisys

Investigations on Target Tracking and Classification Using Multiple Sensor Data Fusion

Task IV - Evaluation of Hardware/Software Processing Architectures

Task V - Study of Displays and Man-Machine Interface

Technical Report / Rev. -

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FOREWORD

PARAMAX submits this report as the Task IV and V combined Draft Report under the provisions of contract number W7701-0-3201/1-XSK.

This document is organized as follows:

- **EXECUTIVE SUMMARY**
- **TASK IV REPORT (DRAFT) - EVALUATION OF HARDWARE/SOFTWARE PROCESSING ARCHITECTURES**
- **ANNEX A - EVALUATION OF COMPUTER PROCESSING TIME**
- **TASK V REPORT (DRAFT) - STUDY OF DISPLAYS AND MAN-MACHINE INTERFACE**
- **LIST OF ACRONYMS**

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EXECUTIVE SUMMARY

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EXECUTIVE SUMMARY

This Technical Report is presented by PARAMAX Systems Canada (PARAMAX) in response to Services and Supplies Canada (SSC) Contract no. W7701-0-3203/01-XSK for Investigations On Target Tracking and Classification Using Multiple Sensor Data Fusion (MSDF). This study is the fourth analysis to be delivered of the six reports developed for the MSDF project. The contents of this report fulfil the technical requirements of Task IV, "Evaluation of Hardware/Software Processing Architectures", and of Task V, "Study of Displays and Man-Machine Interface", as specified in the PARAMAX Technical Proposal developed in response to Defence Research Establishment Valcartier (DREV) Technical Specification No.1121-90-9.

The goal of Task IV of this project is to define a hardware configuration for both a general purpose processor and a parallel processor, to define a set of MSDF benchmark algorithms based on the knowledge of the MSDF problem in the work performed in Tasks I, II, III and other Unisys Data Fusion Studies, and to analyze the performance of each of the algorithms in the context of the target architectures.

The analyses in the Task IV report are aimed at developing an understanding of hardware and software implementation issues for a high performance fusion function within the Anti Air Warfare (AAW) frigate of the year 2000. The AN/UYK-507 CB computer is selected for the study of the general purpose processor implementations. An extended parallel processing architecture is proposed within the militarized AN/UYK-507 VME computer, capable of executing approximately 100 Million Operations per Second (MIPS), for the study of the parallel processing implementations. A central level fusion function using the Multi-Hypothesis Tracking (MHT) method is selected for the study of benchmark algorithm implementations.

The goal of Task V of this project is to document and discuss the Operator-Machine Interface (OMI) aspects of MSDF processes and systems identified during the Literature Survey and to categorize the discussions in terms of Integrated Real-Time Displays; Automated Fusion Processes as Decision Aids, and Database Management and Query Languages.

The analyses in the Task V report focus mainly on the OMI issues of an AAW frigate employing the central-level fusion function using the MHT method discussed in Task IV. This report also includes a discussion of Human Factors studies for the Canadian Patrol Frigate (CPF) and identifies OMI aspects that have been of particular interest to the Canadian Naval Forces.

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TECHNICAL REPORT - Rev. -

TASK IV - EVALUATION OF HARDWARE/SOFTWARE PROCESSING ARCHITECTURES

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Task IV: Evaluation of Hardware/Software Processing Architectures

The objective of this contract is to undertake a study of Multiple Sensor Data Fusion (MSDF) techniques and issues, to analyze, evaluate and propose data fusion algorithms integrating data acquired from dissimilar sensors within the same platform, to study and select the Hardware/Software environment supporting these algorithms, to propose Research and Development topics related to the MSDF domain based on the above analysis, and to analyze the feasibility of MSDF implementations.

This study is the fourth analysis to be delivered of the six reports that are performed to accomplish the objective of this contract. The objective of this task (Task IV) is to evaluate the hardware/software processing architectures for the implementation of a high performance MSDF function. This evaluation is based on the detailed understanding developed during Task III of the complexity and type of algorithms necessary to provide an MSDF capability to the Advanced Anti Air Warfare (AAW) Frigate described in Task I. It consists of the following sections:

1. Candidate Architectures
2. General Purpose Processor Architecture
3. Parallel or Concurrent Computer Architecture
4. Selection of Benchmark Algorithms
5. Study of the Implementation of the Algorithms
6. Concluding Remarks

The Candidate Architectures section reviews a number of different computer architectures, and identifies and selects the general purpose and the parallel (or concurrent) computer architectures that are used for the study of implementation of MSDF algorithms.

The General Purpose Processor Architecture section describes in detail the design of the selected general purpose computer. The level of detail included is necessary to provide the reader with the requisite understanding of the hardware (HW) components within a processor for the discussion of the parallel computer architectures.

The Parallel or Concurrent Computer Architecture section proposes a computer architecture where multiple processors are connected to a bus, allowing parallel implementations of MSDF functions to increase its performance.

The Selection of Benchmark Algorithms section describes an MSDF algorithm, expected to be most

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processor resource demanding, to be used as a benchmark for evaluation of implementations of MSDF within different processors.

The Study of the Implementation of the Algorithms section evaluates the time required to execute the selected benchmark algorithms within both general purpose and parallel computer architectures. For the parallel computer architecture a specific software implementation is selected to maximize the parallel execution of the software.

This report mainly concentrates on two computers and one (most processor resource demanding) MSDF benchmark algorithm. The analyses in this study will develop a solid understanding of complex MSDF algorithms and their implementation within general purpose and parallel computer architectures. This knowledge can be easily generalized for implementation of fusion processes within any new computer architectures that may be available in the future.

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IV.1 Candidate Architectures

Task II and III analyses established that one of the most significant constraints for implementing sophisticated, high performance MSDF systems has been the processor resource availability. Task II described a large number of existing fusion systems which selected a lower performance fusion architecture (sensor-level) only because of the processor limitations. Task III established a detailed understanding of algorithms within different MSDF architectures. Of these architectures, the one which will benefit the AAW Frigate the most is the central level fusion architecture, which is anticipated to require capabilities beyond any of the currently available militarized processors. For the implementation of such an architecture, a computer with parallel processing capabilities would be required. The fusion architecture most likely to be achievable within a general purpose processor is the sensor-level fusion.

The analyses in this report are for the most part aimed at learning and understanding the data fusion hardware (HW) and software (SW) implementation issues within general purpose and parallel processors for an AAW frigate. Hence the criteria for selecting the processor(s) will focus on finding well understood high performance computers appropriate for naval applications rather than the best general purpose and parallel processing computers in the high tech industry.

This section reviews the various processor architecture studies ongoing within PARAMAX Systems Corporation from the perspective of suitability for application in the MSDF architectures discussed in Task III. The following candidate architectures have been examined:

1. The AN/UYK-507 processor designed and developed by the Paramax Information Products Group (PIPG) in Winnipeg, Manitoba, to support the CPF/SRP II and TRUMP programs;

2. The extension of the AN/UYK-44(V) Industry Standard Architecture (ISA) which supports Versa Module Eurocard (VME) bus functions and multiprocessor capabilities, designed by Electronic Information System Group (EISG), PARAMAX Systems Corporation;

3. The 68020 based processor called the Information Processing Unit (IPU), also developed by PIPG for the New Shipborne Aircraft (NSA) program;

4. A number of other 680x0/VME based systems used in different PARAMAX Systems Corporation programs;

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5. The Layered Network Advanced Computer Architecture developed and patented by EISG.

In various benchmark tests (performed by PIPG) among the different general purpose processors used in PARAMAX Systems Corporation, the AN/UYK-507 processor was proven to be superior. It greatly outperforms the MC68030 (more advanced than 68020), the AN/UYK-44, the AN/UYK-20 (AN/UYK-505) and the AN/UYK-502 computers in every one of the coordinate conversion, matrix inversion, requantization and various steering control algorithm benchmark tests. Hence this processor is selected as the general purpose processor discussed in this study. An additional advantage of selecting this computer for this study is that it is the processor on most Canadian advanced naval platforms and at the Combat System Test and Support Facility (CSTSF) at PARAMAX, and the results of these analyses will be directly applicable to the future implementation of fusion in these environments.

Of the parallel processing architectures under development at PARAMAX Systems Corporation some are evaluated inappropriate for the implementation of the central level fusion architecture for the AAW Frigate because of insufficient processing capability, and some because the technology is not sufficiently developed and understood (e.g., Layered Network Architecture). This report proposes a new expanded hardware configuration for the AN/UYK-507 general purpose computer using a VME bus based for concurrent or parallel processing (AN/UYK-507 VME computer).

The detailed configuration and performance characteristics of the general purpose processor and parallel processing architectures is discussed in the following sections.

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IV.2 General Purpose Processor Architecture

For military applications, the AN/UYK-20 (or AN/UYK-505) computer was upgraded to the AN/UYK 502 and the AN/UYK-44 computers, where the latter uses a Common Bus (CB) architecture. Further upgrades were made to improve the performance of these computers for military applications. In particular, EISG in St-Paul and PIPG in Winnipeg developed, in a joint project, a new chip set to improve computer performance for real time applications; that is, the 507/44 Enhanced Processor (EP) chip set [Unisys Winnipeg, 1988; Unisys Winnipeg, 1991a].

The AN/UYK-507 militarized computer has shown its high performance in data processing as compared to other militarized computers of the series 500. Furthermore, the 507 chipset design can also be used for new architectures; such as concurrent or parallel processing.

IV.2.1 507 Processor General Description

The general architecture of the 507 Central Processor (CP) is shown in Figure IV.1. The CP is composed of the Instruction Processor (IP), the Cache Controller (CC) and the Bus Interface Unit (BIU) [Unisys Winnipeg, 1991a & b; Sperry St-Paul, 1991].

The IP is a single chip processor that is micro-code-controlled by external micro memory. It controls the instructions to be processed. The IP has two primary external interfaces. The first one is the micro memory interface which supports a 16-bit (32 K word memory) address and 64 bits of data that work along with the micro code block to decode some instructions. The second external interface is the processor instruction/data interface which interfaces with the CC and supports four stages of pipelining.

The IP consists of eight major functional blocks with a full 32-bit architecture. These are: the microsequencer which provides the interface with the micro memory; the arithmetic unit that operates on 32-bit integer or floating point operand; the multiply unit; the divide unit; 32 general purpose registers; an address generator; an 8 entry, 16 bit wide instruction queue; and P-history and breakpoint hardware support for software debug.

The CC manages the Cache Memory (CM) array. The 64 K-bytes on-board CM serves as a local, high-speed memory functionally dedicated to the CP to increase its effective memory bandwidth. Instructions are stored in cache whenever a new address is referenced (cache miss).

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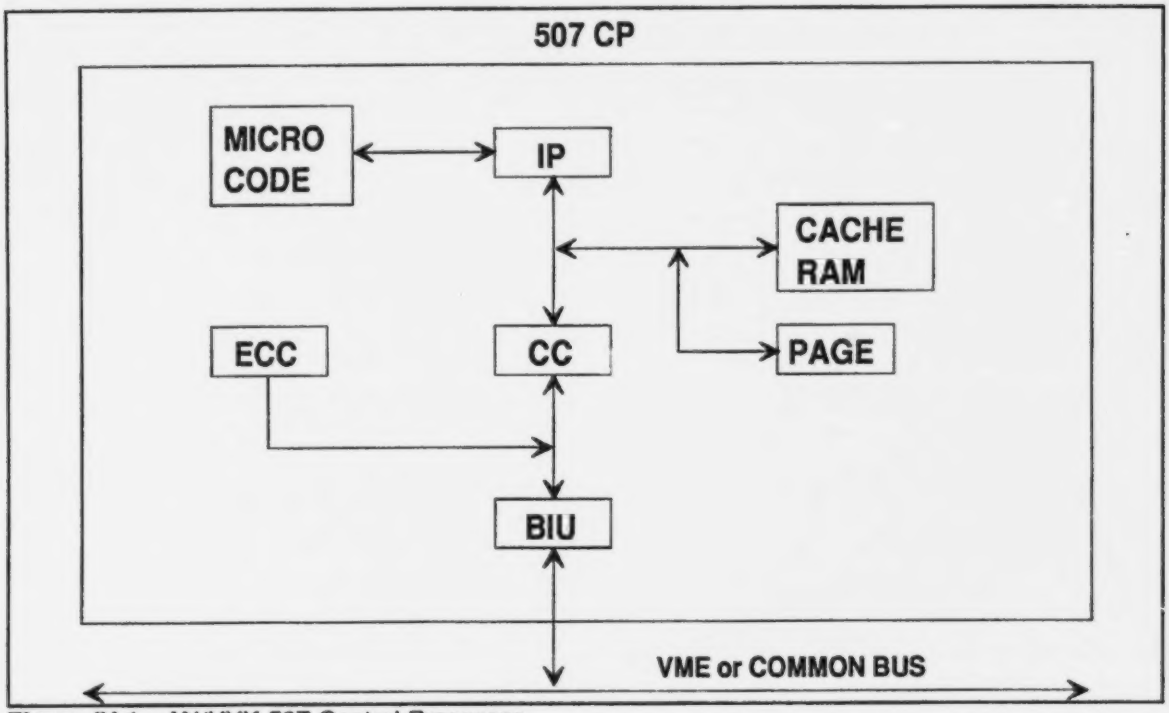

Figure IV.1 AN/UYK-507 Central Processor

The CC makes available to the IP data which is normally resident in the CB memory. The IP can then access this data in less time than would be required for a main memory reference. The CC performs this operation by capturing data requested by the IP in the fast cache Random Access Memory (RAM) so that subsequent reads and writes to the same memory can be made much faster. The CC is also responsible for processing read and write requests from the IP, providing arbitration for CC busses, controlling all page array read and write operations, and self-test of the external cache array and page table.

The BIU has interfaces to the CC and the backplane bus. The BIU interface (BBUS) to the CC carries address/data traffic between the IP and backplane, which is the main memory. This bus also connects to a second CC that eavesdrops on backplane traffic to ensure that cache memory is up to date [Eavedrops Cache Controller (ECC)] . The BIU is the backplane interface which is configurable to support synchronous or asynchronous operation of a standard (16-bit) or an extended (32-bit) CB. Bus arbitration and eavesdropping are supported for both CB and VME bus configurations.

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IV.2.2 507 Chipset Applications

The 507 chipset, which normally resides on the CP card, has been designed to emulate the AN/UYK-502, the AN/UYK-505 and the AN/UYK-44 processors with the appropriate micro code. Thus, the 507 chipset can be used in the AN/UYK-44 CB computer architecture to replace its original processor. The next enhancement to this system is a two-card set 44-EP which can replace the AN/UYK-44 processor, resulting in the AN/UYK-44(EP) CB. Since the 507 chipset can support the VME bus configurations, a new card design resulted in the AN/UYK-44 (EP) VME. The VME bus configuration is explained in section IV.3.

The 507 CP is also used in the general purpose AN/UYK-507 computer architecture. This architecture is described in the following section.

IV.2.3 AN/UYK-507 General Purpose Computer Description

The AN/UYK-507(V) computer has been designed and developed as a cost effective solution for the upgrade of AN/UYK-502 and the replacement of the AN/UYK-505 Data Processing Set (DPS). The 507 is a 16/32-bit general purpose military processor capable of performing 5 Million Instructions Per Second (MIPS) and of being configured to suit many real-time applications. As mentioned above, it is functionally compatible with the AN/UYK-502(V), the AN/UYK-505(V) and the AN/UYK-44 standard military computers, with enhanced processing and memory capabilities. Some other advantages of the AN/UYK-507(V) computer are that it improves the system performance, includes ADA-friendly instructions, and it can be accessible for technology insertion [Unisys Winnipeg, 1991a & b].

Furthermore, there is an enhanced design for the CP of the AN/UYK-507(V) which is expected to increase the performance of this general purpose computer to about 7 MIPS.

IV.2.3.1 AN/UYK-507 Computer Architecture

The primary block diagram description of the AN/UYK-507 is shown in Figure IV.2. It consists of the CP, Input/Output Processor (IOP), Memory Interface (MI), Memory Arrays (MAs), Maintenance Processor (MP), Operator Panel (OP) and Input/Output Interfaces (IOIs). There are three well defined busses: the Reconfigurable Modular Family (RMF) I/O bus, the Memory Bus and the Common Bus (CB). This computer is named AN/UYK-507 CB to symbolize its common bus design as shown on Figure IV.2 [Unisys Winnipeg, 1991a & b].

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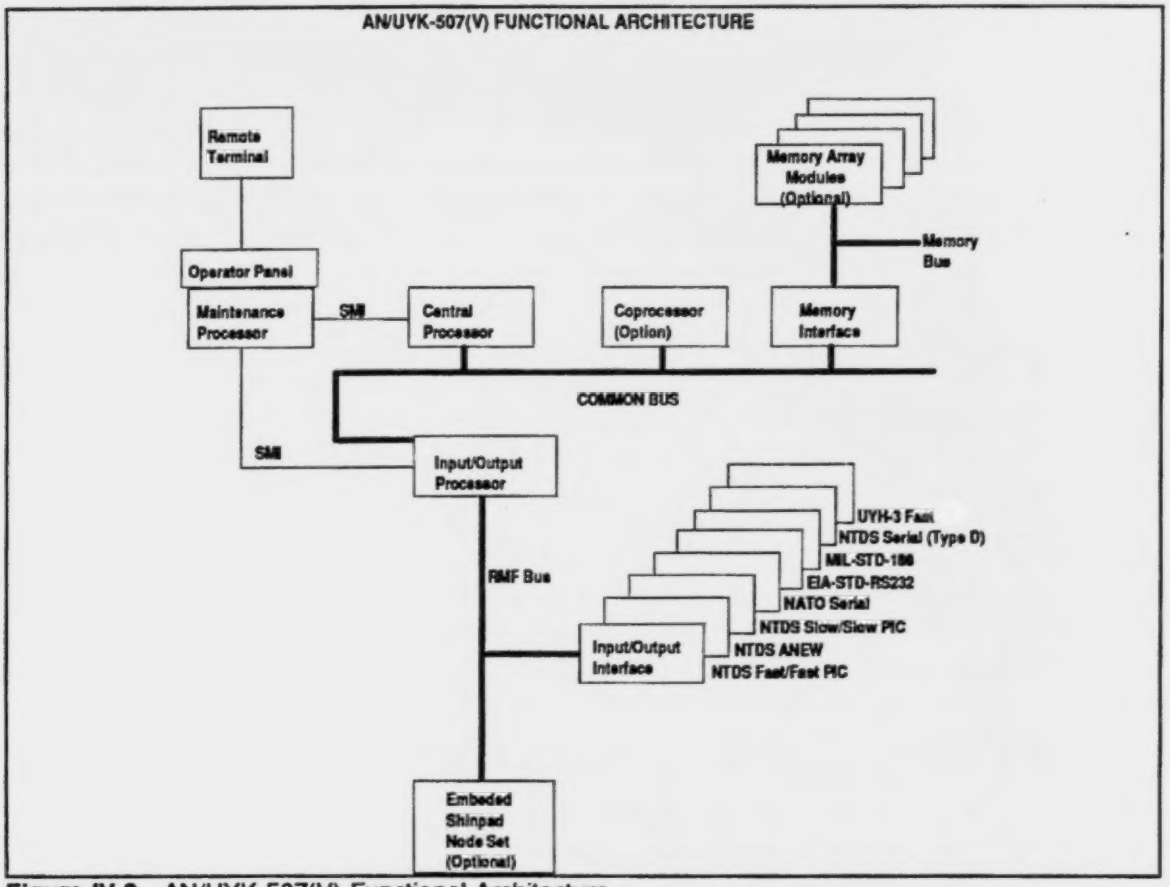

Figure IV.2 AN/UYK-507(V) Functional Architecture

The CP is organized around four Application Specific Integrated Circuits (ASICs) which contain the IP, the CC, the ECC and the BIU as described in section IV.2.1. The 507 CP card has a 64K byte cache memory with a 45MHz clock allowing the processor to perform 5 MIPS. This feature enhances the processing speed above that of the other computers mentioned.

The IOP provides the interface between the RMF bus and the common bus. The IOP executes all I/O commands and chained I/O instructions. It contains a bit-slice processor and a stored microprogram to execute the I/O instruction repertoire.

The MI provides access to main memory for the CP and IOP via the common bus. The MI provides

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access to additional memory cards via a structured memory bus. The MI also provides single-bit error detection and correction, and double-bit detection, for all main memory. The MI provides up to 512K x 16-bit words of SRAM, or 256K SRAM and 256K EEPROM.

The Memory Array Dynamic RAM (DRAM) provides 512K, 1M, or 2 Mx16-bit addressable words of storage. The MA contains the necessary logic to perform automatic refresh of the DRAM cells.

The MP is a micro processor controlled subassembly of the AN/UYK-507 (V) operator panel. The MP interfaces to the internal functions and registers of the CP and the IOP. It also interfaces and monitors the functions of the AN/UYK-507 (V) computer panel and the CP. The MP provides a remote terminal interface capability which provides user remote access and control of the operator panel functions, the CP and IOP internal registers, and the main memory.

The OP consists of the controls and indicators required for operating and maintaining the AN/UYK-507(V).

The IOI provides the interface between the RMF bus and the peripheral equipment as shown in Figure IV.2.

The Serial Maintenance Interface (SMI) transfers data between the MP, CP and the IOP. The SMI is used to transfer built-in test data, to aid in debugging, transfer information between a remote terminal and main memory, reprogram EEPROMs (bootstrap) on the MI via remote terminal, and relay operator panel information to the CP.

The RMF data bus provides an interconnection scheme allowing common communication between IOI modules and the IOP. A multiplexed address/data bus provides the principal medium of communications between subsystems of the RMF bus. It offers a shared interface between processing, storage, and input/output modules thereby providing remote acquisition and distribution of commands, data, and status information.

The CoProcessor (CoP) option is for future growth. A single CoP card can be added to the actual AN/UYK-507 CB for parallel processing. This is because of common bus limitations.

The AN/UYK-507 Common Bus allows communication between the CP, the IOP, the CoP and the main memory interface. This bus implements a 32-bit address and a 32-bit data bus capability. This feature of the AN/UYK 507 CB, among others, allows this computer to process data at a faster rate. The CB is also a fully synchronous, pipelined bus. A CB clock is used to synchronize all signals which

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are transmitted or received via the CB.

The MI Bus allows communication between the MI module and up to 4 MA modules. The Memory Bus provides for memory expansion beyond the base memory resident on the MI module. The MI bus is a fully synchronous bus, using the CB clock to synchronize all signals which are transmitted or received via the bus. The MI Bus provides to the MA modules read and write data only.

IV.2.3.2 AN/UYK-507 CB Computer Architecture for MSDF Applications

The AN/UYK-507 CB will probably support some MSDF applications. For example the sensor-level fusion configuration as discussed in Figure III.4 from Task III Report may be supported. This will be further discussed in section IV.5.1.

However, the AN/UYK-507 CB alone is not capable of supporting the central level fusion data reported by all sensors. This is because central level fusion requires that a very large number of contacts and tracks be processed in a very short time. It is estimated in section IV.5.1 that the AN/UYK-507 CB CP requires 45ms to process contact data from all sensors received during the time interval equal to half the buffer rate of the fastest sensor, the Medium Range Radar (MRR), i.e. 7.8ms, (the MSDF processing interval adopted in section IV.5). This radar processes 128 sectors in one second. The time required to process all the data in one sector is therefore too long. This is explained in more detail in section IV.5.1.

In order to increase the efficiency of data processing for central level fusion, a concurrent or parallel processor architecture was developed (for the AN/UYK 507 VME computer), which is described in the following sections. This Computer design is more efficient for solving MSDF central level fusion problems. The estimate for the 507 VME computer to process the same amount of contact data is 6ms compared to 75ms with the 507 CB.

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IV.3 Parallel or Concurrent Computer Architecture

It was mentioned above (paragraph IV.2.3.2) that a parallel processor architecture is required to implement the central level fusion algorithms of the AAW frigate.

A general definition for a parallel processing computer is one that can perform operations using more than one processor simultaneously. Parallel processing can be defined in three different areas: algorithm and applications, programming language and architecture including hardware, and operating systems [Obermeir, 1988].

Generally speaking, parallel computers are composed of several processors and large memory capabilities. They have the potential to solve problems with vast computational demand. The idea behind parallel processing consists of a number of autonomous processing elements sharing a central memory. Every processing element can read or write one shared memory cell each cycle [Dickey et al., 1986].

Several techniques of multi-stage interconnection network topologies exist to link the processors and memory together in order to implement parallel processing computers. Among them are the utilization of Baseline Network [Wu and Feng, 1981], the Hypercube Network [Hayes, Mudge et al, 1986; Dunigan, 1986; Hayes, 1988], and the Layered Network [Bennet and Shon, 1991]. The latter compares the Layered Networks with other interconnection methods. It seems that this method presents good features such as reasonable scalability, high speed, short latency, efficiency for short messages, inherent fault tolerance, a fast routing algorithm and little interference among logically unrelated requests. Even though these are interesting features, it seems that further study remains to be done in this area to improve the network topology [Obermeier, 1988].

Some interesting papers were found in the literature discussing parallel algorithms and parallel processors for Data Fusion [Allen, Kurien and Washburn, 1986; Klein and Kassis, 1989; Cybenko and Allen, 1987]. Although they conclude that the parallel structure algorithms and parallel computers increase the processing performances (higher speed), further investigation and more work should be done to prove the implementations of parallel structures for MSDF.

Because the parallel structure just described (multi-stage interconnection networks) is still evolving, its implementation within an environment of the AAW frigate is not likely to be achievable before the year 2000. An alternative architecture with respect to the definition given above [Obermeir, 1988] is suggested. The term parallel or concurrent architecture will thus be introduced. Parallel or concurrent

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architecture is one in which several processors can work simultaneously, with local memory on each CP card, resulting in very little shared (common) external memory, and with a communication bus enabling all the processors to talk interface.

The purpose of using a parallel architecture is to increase the processing speed to cope with the large data rates required to achieve real-time performance from the MSDF algorithms described in Task II and III Reports. The two alternatives for parallel or concurrent architecture are the 507 CB computer with an added CoProcessor, and the proposed 507 VME computer. The hardware architecture of these computers is described in the following sections.

IV.3.1 AN/UYK-507 CB Parallel Architecture

With the AN/UYK-507 CB computer, it is possible to add one CoProcessor as was mentioned in section IV.2.3.1. The CB has not been designed to support more than one CoProcessor card because of the Common Bus design. There is also a physical space limitation that restricts this computer to one card.

After the development of the enhanced (7 MIPS) CP card, and assuming that the CoProcessor provides 7 MIPS performance also, there is a possibility of approximately 14 MIPS, less the software management overhead between processors. In this study, the AN/UYK-507 CB plus CoProcessor is estimated to be 10 MIPS overall.

The AN/UYK-507 CB having one CoProcessor is not sufficient for implementation of the central level architecture. It can be a short term solution for processing the MSDF algorithms for the sensor-level fusion configuration. In the future, as sensors improve in performance and more sensors are added to the system, more data will have to be processed. Thus a faster computer will be required. The solution for this problem is to design a new computer architecture. The AN/UYK-507 VME architecture for parallel processing offers that increased speed.

IV.3.2 AN/UYK-507 VME Parallel Architecture

The AN/UYK-507 VME parallel architecture for concurrent processing is developed by combining capabilities of the VME bus, the AN/UYK-44 computer architecture and the VME Card implementation. These topics are discussed below.

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IV.3.2.1 VME Bus

The VME bus is a computer architecture where the VME mnemonic stands for Versa Module Eurocard. The term bus means a computer data path. The VME bus architecture can be used with any processor if it is properly designed [Paterson, 1989].

The reasons for using the VME bus among other popular busses depend on the interesting features it presents which include: low cost implementation, parallel processing, reasonable physical dimension, technology insertion and system high performance capabilities.

The VME bus has a 32-bit address bus and a 32-bit data bus. It performs multiprocessing and can operate up to seven interrupt levels. Both the address and data busses can be dynamically configured allowing system expansion as computer technology grows. The VME bus can also handle data transfers at speeds in excess of 40M bytes per second. This type of bus will therefore be appropriate for the communication between the processor VME cards, the Memory VME cards and the I/O VME cards.

The VME bus uses a master-slave architecture. Functional modules called masters transfer data to and from modules called slaves. Since multiple masters can reside on the bus it is called a multiprocessing bus.

The VME bus modules are connected together by backplanes which can have between 2 and 21 slots. One or two backplanes may be used depending upon the system configuration. The physical dimensions of the VME bus allow the connection of up to 16 VME cards within one computer.

IV.3.2.2 VME Cards

As discussed above, the VME bus can work with any processors. For example, the VME card can be designed with the 507 Chip Set processor or Motorolla 680x0 processors. The choice of the VME Card depends on the required application. For this study the 507 Chip Set is selected as the one exceeding in performance the available militarized processors. Furthermore, since this processor is also in the general purpose computer, the performance differences between the two computers will be more apparent (fewer variables to consider).

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IV.3.2.3 AN/UYK-44 Computer Architecture

The AN/UYK-44EP CB architecture is basically the same as the AN/UYK-507 CB discussed previously. The AN/UYK-44EP works with its own 44 MP and common bus environment. This bus is based on the AN/UYK-44(V) bus baseline 22-bit address and 16-bit data [Sperry St-Paul, 19xx].

The AN/UYK-44EP VME computer architecture has been designed to work with the VME and the 44 MP environments. This type of computer was designed for parallel processing implementation to enhance its efficiency and for future open systems for military applications.

IV.3.2.4 507 Chip Set VME Card

The design of the 507 VME card should be similar to that of the 44EP VME card. The 44EP VME card contains the basic CP, the 44 MP on board and the Multi Processing enhanced BIU.

The 507 VME should contain the 507 MP, the Operator Panel functions and the local memory added to the card. The 507 VME card should also contain the Multi Processing BIUs, as discussed in section IV.3.3.1.

IV.3.3 AN/UYK-507 VME Proposed Architecture

In order to increase the processing performance of the AN/UYK-507 so that the MSDF requirements are met, it is necessary to use a parallel processing architecture. Figure IV.3 shows the parallel architecture for the AN/UYK-507 using a VME bus implementation. The VME bus interconnects the VME cards so that the processors can work simultaneously [Bourassa, 1992].

The CP can work along with CoPs for maximum speed efficiency. It is expected that 16 cards can be physically inserted in an AN/UYK-507 VME unit of which 14 could be CP and CoP cards and two cards exclusively dedicated to I/Os. The I/O cards hooked on the VME bus allow communication with external devices such as sensors. Commercial Off-The-Shelf (COTS) Memory cards can also be hooked on the VME bus for shared memory extension.

A VME NATO Serial card or a VME NTDS Fast card hooked on the VME bus can work along with the AN/UYC 503 NODE 6-card set to communicate with the Serial Data Bus (SDB). Another alternative to this would be the design of a VME single-card node for data communication between the VME bus

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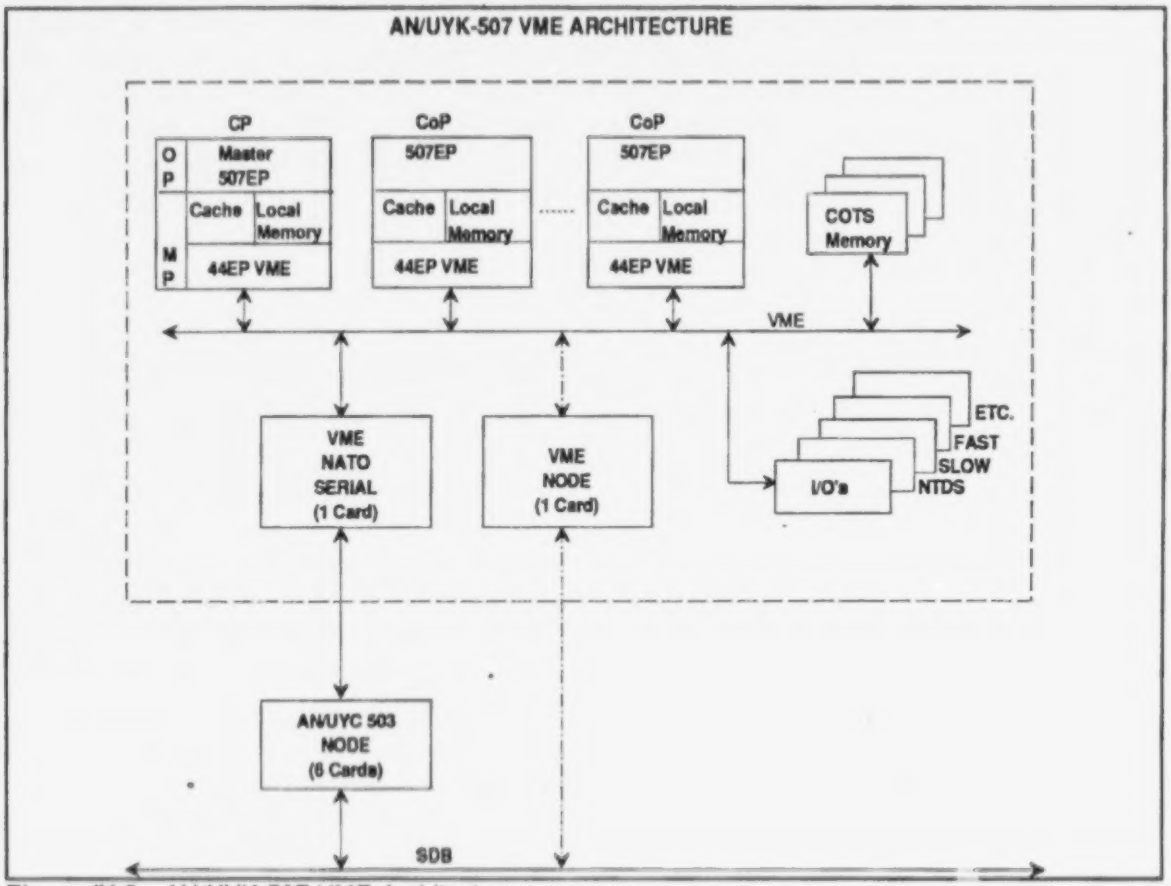

Figure IV.3 AN/UYK-507 VME Architecture

and the SDB.

The idea for the development of this architecture can be understood by the microcode development life cycle shown in Figure IV.4. In A, the MC of the 44 Emulation (44E) and the 44 CB environment with the MP are shown for the AN/UYK-44EP CB computer. In B, the VME environment has replaced the 44 CB environment to lead to the AN/UYK-44EP VME computer. In C, the 507 microcode, the 507 environment and the 507 MP compose the present AN/UYK-507 computer. The idea here is to take the microcode of the 507 in C and merge it with the VME environment of B, resulting in D, the new 507 VME for parallel processing architecture.

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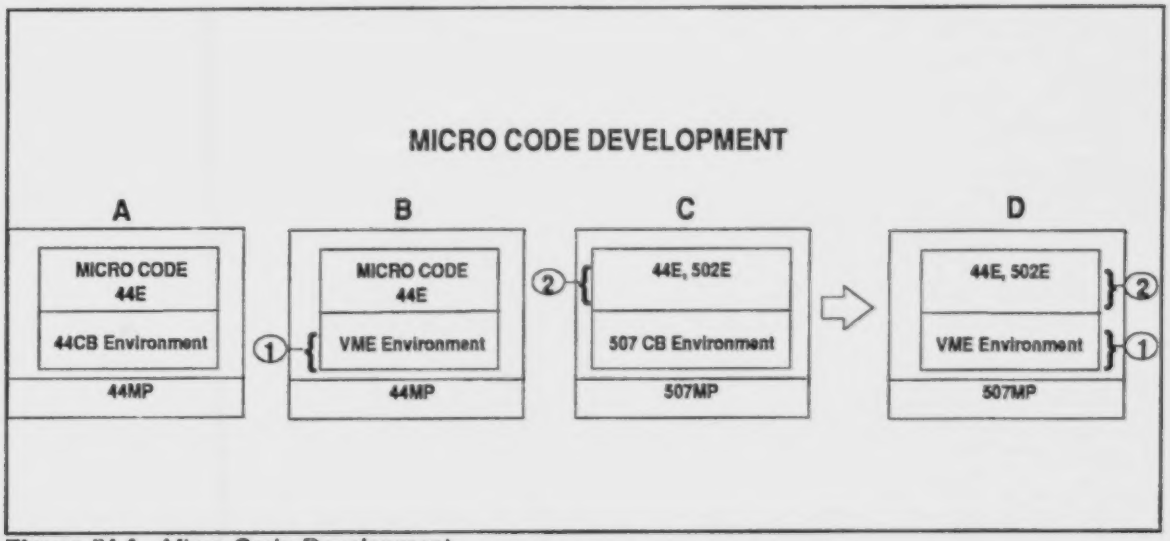

Figure IV.4 Micro Code Development

The extended AN/UYK-507 VME computer that is selected in this study will have the architecture described in Figure IV.3, with an upgraded 507 VME CP, to maximize processing capability. The proposed upgraded 507 VME CP design is discussed in the following paragraph.

As the technology advances, higher performance CPs and CoPs will be developed along with the capability to add more CoPs. However this study selects a parallel processing architecture which is well understood, available by the year 2000, and concentrates on the implementation issues of the central level fusion processes within parallel processing architectures.

IV.3.3.1 Central Processor Upgrades

The proposed upgraded 507 VME CP card design is shown in Figure IV.5. When compared with the 507 CB CP design shown in Figure IV.1, it shows an additional BIU with local memory. The Local Memory is designed to work with the VME environment on the CP card [Bourassa, 1992].

The addition of the Local Memory on the 507 VME CP card would greatly enhance its performance. With a large Local Memory, the data would be processed locally, that is, there would be no need to fetch the data to the External Memory (see Figure IV.5) through the VME bus, thus saving a great amount of processing time. With the current technology and the physical dimension of the VME card, it is estimated that the Local Memory could contain up to 2M bytes of memory.

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In addition to this upgrade, it is anticipated that the present cache memory (64K bytes) should increase by 25%. Further work on the CP is being done on increasing the clock rate by approximately 20% in the near future. Both improvements would increase the present performance.

From the improvements just discussed above, it is anticipated that each 507 VME CP or CoP could reach a performance of up to approximately 10 MIPS.

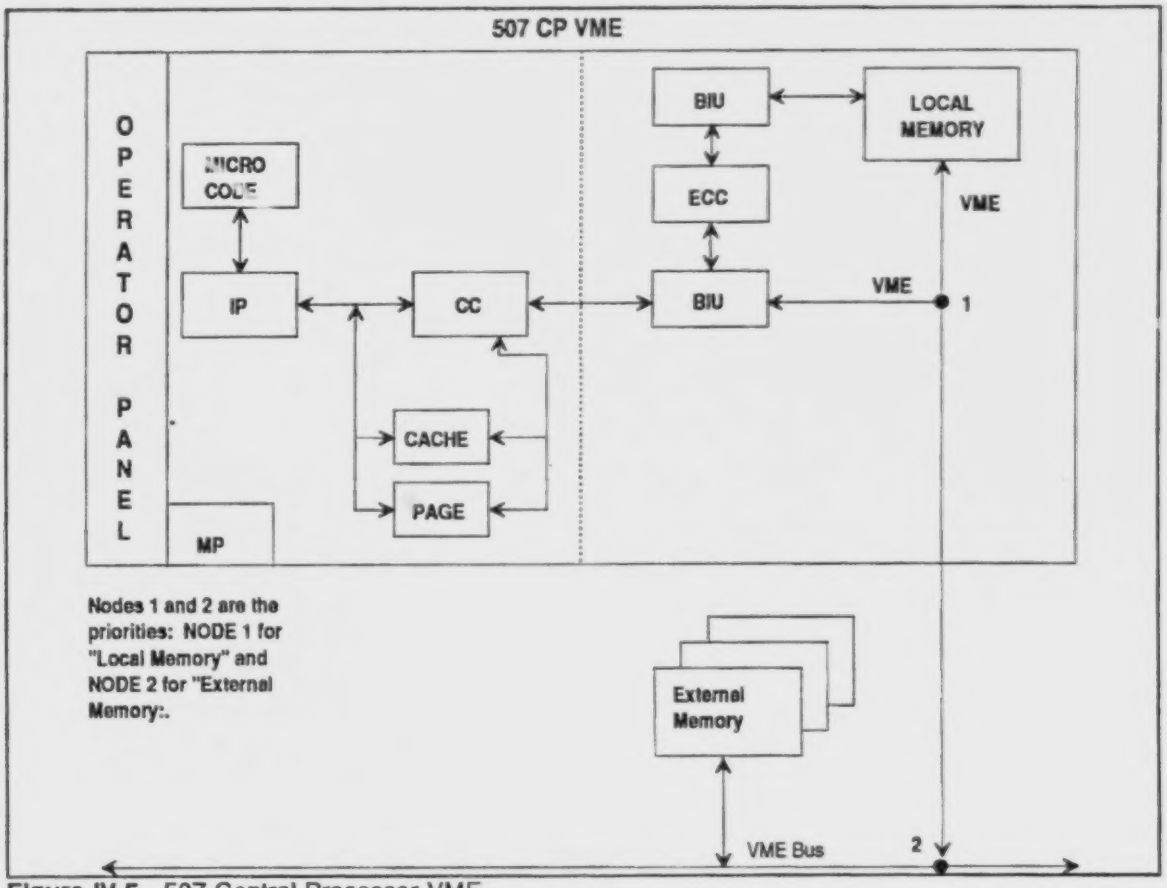

Figure IV.5 507 Central Processor VME

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IV.3.3.2 Expected Overall Performance of the AN/UYK-507 VME Computer

As was mentioned in section IV.3.3, there is a possibility of adding 14 CP or CoP cards in an AN/UYK-507 unit with two I/O cards. Assuming the ideal case of 14 VME (CP or CoP) cards of 10 MIPS each, this would result in a 140 MIPS performance computer (less overhead). Since software is required to manage the data between processors, the MIPS performance degrades, thus reducing the overall processing efficiency of the AN/UYK-507 VME. The software management would therefore play an important role for efficient parallel processing.

The overall performance will vary, depending on the software implementation. The following sections of this report propose one implementation which maximizes the use of parallelism of the most processor intensive central level fusion algorithms, and evaluate the timing of their real-time implementation within the extended AN/UYK-507 VME computer.

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IV.4 Selection of Benchmark Algorithms

The principal purpose of task IV is to determined if a real-time implementation of an MSDF function which has to meet some specific performance and mission requirements is feasible or not. As Task III demonstrated, different configurations lead to better or worse performance but also larger or lesser processing workload. The central level configuration is the most demanding in terms of processing. Therefore, to evaluate the processing workload, the benchmark algorithms will be the set of MSDF techniques and algorithms which perform central level fusion. Being the most complex fusion approach, understanding the implementation issues of these algorithms will establish expertise for evaluation of processing requirements of a fusion function. This set of algorithms is explained in the configuration described in section III.3.2.

Figure III.5 presents a general data fusion function which is an idealization. Some of the proposed algorithms are under development and not yet ready for application; they cannot be considered. They are the pattern matching from the target model identification process and the estimate probability from the attribute fusion process. Also the possibility to process data from other sources will be excluded from the set of benchmark algorithms since this is not usually part of the fusion function that fuses data from sensors onboard a single platform. This eliminates the need of Bearing Intercept Fix (BIF) function. Figure IV.6 below describes with more details the data fusion function which represents the set of benchmark algorithms. This proposed MSDF function is structured in four processes: the data alignment, the data association, the state estimation and the identity estimation. In addition, the database and the man-machine interface complete the design. The algorithms to which parallelism can be implemented are shown with thick line contour boxes. The intrinsically sequential algorithms are represented by regular boxes. For reasons of clarity, the functional diagram outlines only the main fusion processes (involving certain techniques and algorithms). The following sections describe these main processes separately.

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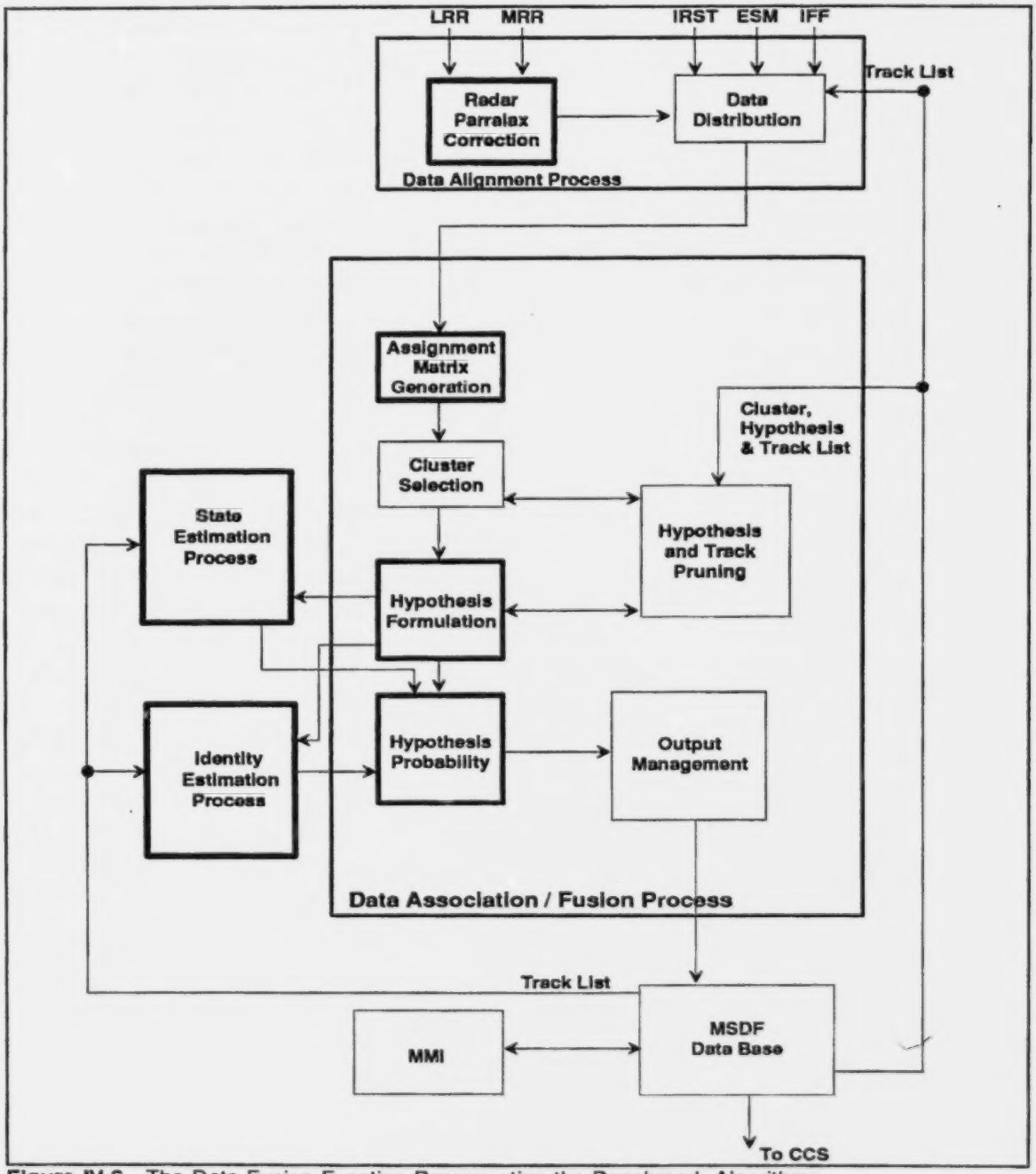

Figure IV.6 The Data Fusion Function Representing the Benchmark Algorithms

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IV.4.1 Alignment Process

The data alignment process performs the functions of spatial and time alignment. First the radar data are transposed in the Infra-Red Search Track (IRST) coordinate system of reference. This function can be implemented in parallel for each radar report since they can be transformed independently of each other. The Medium Range Radar (MRR) reports are transformed using the equations III.1 to III.3 while the Long Range Radar (LRR) use III.1 and III.2. The transformed radar contacts, the Electronic Support Measures (ESM) and the Identification Friend or Foe (IFF) contacts are sent to the data distribution function. This function performs a time alignment to link the sensor data which come usually in "buffers" at some specific frequency to the MSDF function. For this study, it is assumed that MSDF utilises Track-While-Scan (TWS) philosophy, i.e., the sensor data arrives at MSDF at regular intervals as the sensor regularly scans a predetermined search volume [Blackman, 1986], and is processed as it arrives. The observed area is divided into sectors and the contact data must be received by the fusion function in groups called "MSDF buffers". The role of the data distribution function is to prepare the MSDF buffers and to distribute the data of these buffers into the appropriate sectors under process. This task is essential in order to schedule the TWS process. This function also selects the MSDF tracks, hypotheses and clusters pertaining to sectors being processed.

IV.4.2 Association Process

The association process is the cornerstone of the fusion function. It performs the task of selecting the various ways the received information can be combined with the existing MSDF data through the formation of clusters, hypotheses and tracks lists.

IV.4.2.1 Assignment Matrix Generation

The process starts by propagating certain tracks of the track list to the time of certain contacts. The MSDF tracks which belong to the appropriate sector will be propagated to the time of the contacts of the sector under process. This can be implemented as a parallel operation, for each track, which is performed using equations III.5 and III.6. Here, for simplicity, it is assumed that all the targets are described with the same target model. This propagation function prepares, in fact, the data for the generation of the assignment matrix. The elements of the assignment matrix are obtained from this

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general expression [Bar-Shalom 1990, chapter 6; Blackman 1986, chapter 9]:

$$C_{ij} = 2\ln\left[\frac{P_D}{(1-P_D)\sqrt{(2\pi)^{M_{ij}}\beta^2_j V^2_{ij}\det(U_{ij})}}\right] - d^2_{ij} + 2\ln\left[\frac{P(Z_j \mid \hat{Z}_i)}{P(Z_j \mid NewTarget)}\right] \qquad \text{(IV.1)}$$

where d_{ij} and U_{ij} are given according to equations III.7 and III.8. The variable Z_j stands for the attribute information provided by the sensor, while $\hat{Z}_i$ stands for the attribute estimated by the identity estimation process for the track i. M_{ij} is the common dimensionality between the track and the contact, V_{ij} is the volume (generalized) of the measured quantities (range, azimuth or elevation) which appear in the measurement vector $_j$ but which are not included in the track state vector $_i$, and β_j is the density of new targets. C_{ij} signifies the likelihood of the association between contact j with track i. If certain values for C_{ij} are lower than a specific threshold, the association can be declared an uncorrelated event. This is the first simplification rule of the hypothesis generation that can be utilized. This process can also be implemented in parallel since every C_{ij} is independent of each other.

IV.4.2.2 Cluster Selection

The next function of the association process will use the results of the assignment matrix to create new clusters or merge some clusters together. At this point the only new clusters which are created are individual reports which do not associate with already existing tracks. The merging happens when one or more reports join two or more unconnected clusters. The example sketched in Figure IV.7 and the assignment matrix shown in Table IV.1 present a typical situation. In the figure one LRR and four MRR contact are received in tracking sector n. The MSDF function uses the track-while-scan mode. Six tracks in adjacent sectors n+1 and n-1 and in sector n have been selected to be associated with the five contacts. The values of each element C_{ij} in table IV.1 do not necessarily come from the application of equation IV.1. They have been selected for presentation purposes within appropriate realism. Table IV.2 shows typical values of the C_{ij} elements of the assignment matrix. A zero value indicates that a pair of data has a very small probability of association and is evaluated as an uncorrelated event. In multiple sensors data fusion there is a possibility that two contacts of the same "MSDF scan" will associate. The assignment matrix is built to account for this possibility. An assignment coefficient is computed from an expression similar to equation IV.1 with some modifications. The table also indicates to which cluster, among the MSDF cluster list, the selected tracks belong. Table IV.1 represents the output of the assignment matrix box which is transmitted to the cluster selection function. The role of the cluster selection function is to find the sub-matrices which are independent of each other. The results expected from the cluster selection function when it receives the data of Table IV.1 are shown in Table IV.2.

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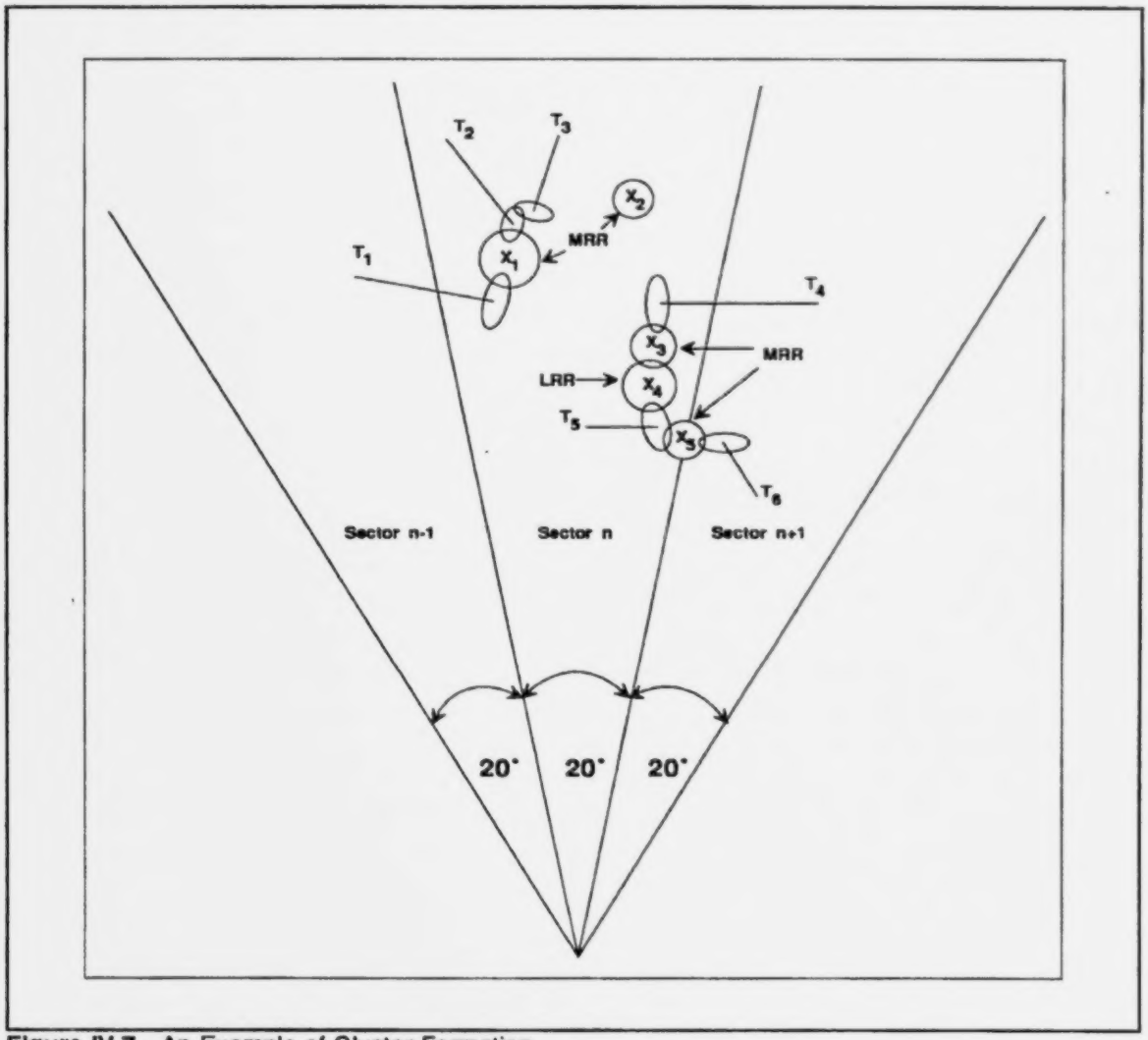

Figure IV.7 An Example of Cluster Formation

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Table IV.1. An Example of a Typical Assignment Matrix for Multiple Sensors

Tracks	Clusters	X_1	X_2	X_3	X_4	X_5
T_1	1	4	0	0	0	0
T_2	2	5	0	0	0	0
T_3		0	0	0	0	0
T_4	3	0	0	3	0	0
T_5	4	0	0	0	4	4
T_6	5	0	0	0	0	3
X_1		6	0	0	0	0
X_2		0	8	0	0	0
X_3		0	0	8	2	0
X_4		0	0	2	7	0
X_5		0	0	0	0	7

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Table IV.2. Cluster Rearrangement of the Assignment Matrix

Tracks	Clusters	X_1	X_2	X_3	X_4	X_5
T_1	1	4				
T_2		5				
T_3		0				
X_1		6				
X_2	2		8			
T_4	3			3	0	0
T_5				0	4	4
T_6				0	0	3
X_3				8	2	0
X_4				2	7	0
X_5				0	0	7

The table indicates to which new clusters the already existing tracks and the received contacts belong. Since the mode of operation of the MSDF function uses tracking by sector, the tracks listed in the submatrix are not necessarily all the tracks of the rearranged cluster but rather the portion which belongs to the sector being processed. As indicated in Table IV.2, the previous clusters 3,4 and 5 have been merged to form a new and bigger cluster. The merging of new clusters can overpopulate the already existing hypotheses list. An algorithm which prunes hypotheses must be included with the cluster selection algorithm to rearrange the hypotheses list. This algorithm is explained below. The selection of the cluster is a sequential process but each new cluster is independent and the rest of the Multi-Hypothesis Tracking (MHT) processing can be performed in parallel for each cluster.

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IV.4.2.3 Hypothesis Formation

The hypotheses list is constructed from the submatrices by the hypothesis formation function. For each selected cluster, the hypothesis formation function combines the existing MSDF tracks with the new received contacts. If the number of suggested new hypotheses becomes larger than a specific limit, the pruning hypotheses and tracks function must withdraw some existing low likelihood tracks.

This function is more complicated in a multiple sensors system since it has to consider association rules which take into account the specifics of the dissimilarity among the sensors. These association rules are discussed in section II.2.2.3.2 of Task II. For example, with the IRST, due to its high target resolution capability and range ambiguity, many IRST contacts of the same scan can be associated to a single MSDF track. This has the disadvantage of increasing the number of plausible hypotheses. For example, the top part of Figure IV.8 shows three reported IRST contacts which can be associated to one MSDF track. The bottom part of Figure IV.8 shows three radar contacts which can be associated to one radar track. Table IV.3 lists the eight hypotheses which can be formulated to explain the tactical situation for the multiple sensors case and the four hypothesis in the single radar sensor situation (or multiple similar radar sensors).

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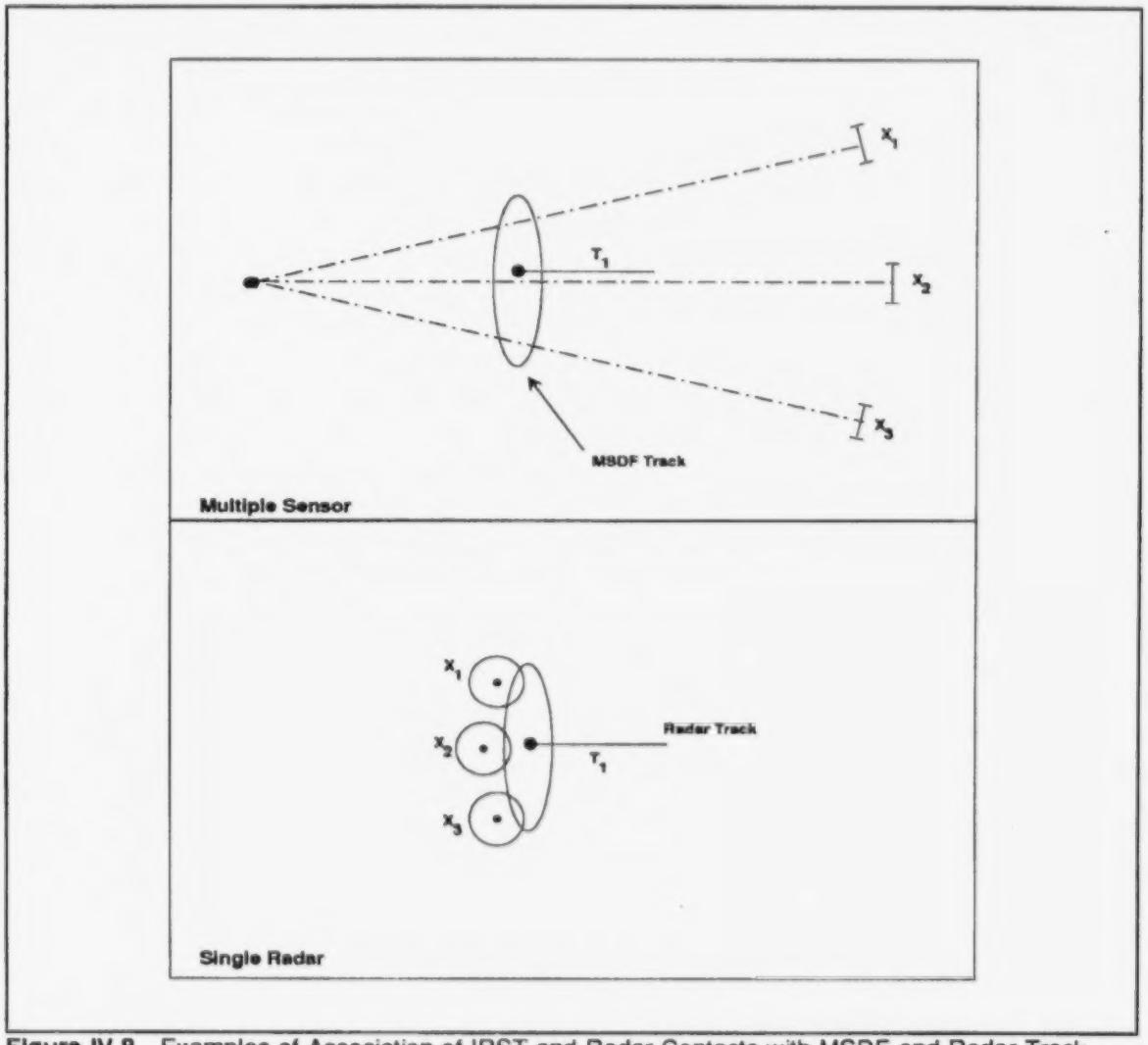

Figure IV.8 Examples of Association of IRST and Radar Contacts with MSDF and Radar Track

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Table IV.3. Example of Hypotheses Formation

Hypothesis	Multiple Sensors		Single Radar	
	Tracks	New Tracks	Tracks	New Tracks
1	T_1	X_1, X_2, X_3	T_1	X_1, X_2, X_3
2	$T_1 + X_1 \rightarrow T_2$	X_2, X_3	$T_1 + X_1 \rightarrow T_2$	X_2, X_3
3	$T_1 + X_2 \rightarrow T_3$	X_1, X_3	$T_1 + X_2 \rightarrow T_3$	X_1, X_3
4	$T_1 + X_3 \rightarrow T_4$	X_1, X_2	$T_1 + X_3 \rightarrow T_4$	X_1, X_2
5	T_2, T_3	X_3		
6	T_2, T_4	X_2		
7	T_3, T_4	X_1		
8	T_2, T_3, T_4			

In the second and fourth columns of Table IV.3, the plus sign indicates that track T_1 is updated with the contact data and the arrow indicates that a new number is assigned to the updated track. The third and fifth columns show the unassociated contacts which can be tentatively established as new tracks. The single radar situation leads to the formation of four hypotheses. These same hypotheses also appear in the situation of multiple sensors but, in addition, there are four others which consider the possibility that the MSDF track represents two or three closely spaced targets. If the MSDF tracks have some attribute information and the IRST contacts also contain some attribute information, it is possible that the number of hypotheses will be reduced by the attribute portion of the criteria shown in equation IV.1.

IV.4.2.4 Hypothesis and Track Pruning

Hypothesis formation and cluster selection are connected to the function of hypothesis and track pruning. Called by the cluster selection function, this function prunes the low probability tracks of the track list when too many hypotheses exist in the cluster obtained from the merging of two or more previous clusters. When called by the hypothesis formation function, the pruning function deletes the existing MSDF low likelihood tracks (or contacts). This is done because the MSDF function has to

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limit the number of generated hypotheses and tracks a some specific threshold.

This function is essentially a pruning process which controls the number of tracks and consequently the number of hypotheses. Some merging of similar tracks could be performed also but this operation is processing intensive. Merging of similar tracks is performed at the end of the MHT algorithm. As mentioned in [Blackman, 1986 chapter 14] there are two thresholds in the control of the number of tracks and hypotheses. The MHT should be capable of retaining M_1 hypotheses (i.e., at the end of the MSDF function) and M_2 hypotheses at the contact processing level (i.e., at the end of cluster selection and hypothesis generation algorithm). M_2 is larger than M_1 and its values are a function of the computing architecture and performance for M_2 and human factor consideration for M_1. In principle, the MHT algorithm must also consider thresholds on the number of tracks at both levels, NT_1 and NT_2. Both thresholds must be respected for each level.

IV.4.2.5 Hypothesis Probability

This function uses the hypothesis content from the hypothesis formation function and the measurement updates from the state and identity estimation processes to evaluate the normalized probability of the hypotheses within each cluster. The computation is performed using equations of the equation III.13 type. Equation III.13 is specifically suited for active sensors. Since the MSDF function deals also with passive sensor contacts, a modified version should include the particularity of the passive contacts. It is shown that the expression for passive sensor reports is only a bit less demanding on computation [Reid, 1979]. For the moment more investigations must be made to define the correct way to compute the normalized probability in including the passive as well as the active contacts. This report (section IV.5) addresses the computer processing required by the set of benchmark algorithms. The use of equation III.13 in the evaluation of the processing power will provide a maximum limit.

IV.4.2.6 Output Management

The last step, after evaluating all the hypotheses within each cluster, is the clean up of the results. If the last measurement update of young tracks has split a cluster into distinct clusters, then the output management function has to redesign the cluster list and renormalize the subsequent hypotheses list. After this operation is performed the number of hypotheses and tracks in each cluster must not exceed the allocated limits of M_1 and NT_1 respectively. The tracks in a cluster can be more numerous than NT_1 if there is high target density but they cannot exceed NT_2 due to the control performed by the pruning function previously discussed. To reduce the number to NT_1 the function will first combine the

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similar hypotheses, and if necessary the function will prune the lower probability hypotheses until the limits of both are reached. The similarity of two hypotheses a and b can be determined if both hypotheses have the same number of tracks and if all the tracks pertaining to each hypothesis have similar identity and positional information related as follows:

$$| x_{ai} - x_{bi} | \leq \beta \sqrt{\sigma_{aii}^2 + \sigma_{bii}^2} \qquad \text{(IV.2)}$$

$$\gamma^{-1} \leq \frac{\sigma_{aii}^2}{\sigma_{bii}^2} \leq \gamma \qquad \text{(IV.3)}$$

where i=1,2...6 and where the x and the σ represent the state vector components and the diagonal element of the covariance matrix. It is suggested that the phenomenological parameters β and γ be equal to 0.1 and 2 respectively [Blackman, 1986; Reid, 1977]. As an alternative, these parameters can be dependent of the target density and raised until the limits M_1 and NT_1 be reached. If both hypotheses comply with the similarity test the one with the lowest probability can be pruned or, instead, the positional information of the tracks can be combined according to:

$$\vec{X} = \frac{Pr(a)\vec{X}_a + Pr(b)\vec{X}_b}{Pr(a) + Pr(b)} \qquad \text{(IV.4)}$$

$$P = \frac{Pr(a)P_a + Pr(b)P_b}{Pr(a) + Pr(b)} + \frac{Pr(a)Pr(b)}{[Pr(a) + Pr(b)]^2}(\vec{X}_a - \vec{X}_b)(\vec{X}_a - \vec{X}_b)^T \qquad \text{(IV.5)}$$

The identity information is combined using an expression similar to equation II.53 as will be explained later. Finally, it is possible that combining and pruning could split a cluster into disjoint clusters. Therefore, a last rebuilding of the cluster list will be necessary with the appropriate hypothesis normalization.

IV.4.3 State Estimation

Various algorithms exist concerning the estimation of the target state and covariance matrix. The most standard one is the cartesian linear adaptive Kalman Filter. As a benchmark algorithm this Kalman filter will be used. The set of equations of this filter are described in section II.2.7 of Task II.

Other algorithms which take into account the unlinearity or which use parallel filtering principle are

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preferable. However for this task it is more important to verify the validity of the MHT data association method for MSDF within a specific processing architecture. If this set of benchmark algorithms shows that central level MSDF is feasible, the extension to high performance filter algorithms would not increase the processing significantly and could be considered in subsequent studies.

IV.4.4 Identity Estimation

The identity estimation process has to estimate target identity using sensor-measured attributes in the context of multiple sensor fusion utilizing the Dempster-Shafer evidential theory. The tracks to be updated and the new tracks to be initialized are processed by the identity estimator function. In this proposed MSDF function, a track is a generalised object which includes not only state and covariance but also information relative to the identity. This information is under the form of a list of propositions with corresponding belief, support and plausibility as shown in Table IV.4 below. The proposition A_i represents typical identity (e.g., U.S. Frigate, commercial aircraft Boeing 747, CF-18, ASW Helicopter EHI-101, etc...). Theoretically the identity estimation approach should provide a degree of belief (and consequently a support and plausibility) for target types of the threat database. In principle, a typical threat database is made up of 25,000 entries and only the most significant propositions are kept in the tracks. The rest are attributed to the ignorance parameter Θ. The content of the threat database is the subject of future development. An exhaustive threat database must contain all the types and classes of military and commercial radar, aircraft, ship, etc... which are likely to be detected.

Table IV.4. Example List of Propositions for Identity Estimation

Proposition	Belief	Support	Plausibility
A_{14}	0.76	0.76	0.86
A_{43}	0.08	0.08	0.10
A_{783}	0.07	0.07	0.11
A_{12086}	0.04	0.04	0.05
Friend	0.03	0.98	0.99
Surface	0.01	0.97	0.99
Ignorance (Θ)	0.01	1	1

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The literature about MHT within multiple sensors does not address the impact of the identity estimation in the evaluation of the feasibility of the MHT method. In the following sections these impacts are to some extent identified and quantified. Previous tasks (II and III) have shown that the Dempster-Shafer evidential approach is slightly favoured over the Bayesian approach. Therefore the evidential approach is suggested as set of benchmark algorithms for the process of identity estimation. Equations II.53, II.54 and II.56 explained in section II.2.5 of task II represent the basic equations of the algorithm.

IV.4.5 MSDF Database

The output data of the MHT algorithm is divided into three lists: a track list, a hypotheses list and a cluster list. This data is broadcast to all the processes of the MSDF function and to external functions such as CCS and MMI. The track list is communicated to all processes while the hypothesis and cluster list are sent only to the data association process through the pruning algorithm.

The track list tracks are made of positional information, identity information and status information. The positional information consists of the time of the last measurement update, the state vector, the covariance matrix and certain previous contacts (depending on the performance requirement) which were used to update the tracks. A track probability or a score can also be included in the positional information. The identity information is a list of potential identities or attributes with appropriate level of confidence (degree of belief, support and plausibility). The status information consists of details about the status of the tracks (potential, tentative, confirmed, other), the number of consecutive "misses" , track quality, a reference count number which indicates the number of hypotheses that have this track, and a track number.

Each hypothesis of the hypotheses list has three components: a probability or a score, a hypothesis number and a pointer list which is related to a subset of the MSDF track list. The clusters of the cluster list are simply made of two lists of pointers; for the tracks and the hypotheses pertaining to them.

IV.5 Study the Implementation of the Algorithms

This chapter analyzes the processing workload performed by the dedicated processor to run the benchmark algorithms. To gauge the real-time capability to run the algorithms, the time required to perform a cycle of the MSDF function must be estimated. A quantification of the processing work

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requires that the performances and design requirements of each algorithm be exactly specified. In other words the algorithms should be completely structured and ready to be implemented. There are many parameters, secondary functions and specifications in the proposed benchmark algorithms which have not been addressed. Examples of such parameters are the limits M_1, M_2, NT_1 and NT_2. Although formal simulation analysis is necessary to evaluate real capability, within this study it was evaluated that more understanding about the implementation of a central level fusion function using the MHT method can be established by making realistic assumptions, from which rough estimation of the processing time to run a cycle is obtained.

There are a number of alternative methods to implement a central-level MHT fusion. The one, where each sensor buffer is fused as it arrives and the one where the MHT scans with a period equal to half of the fastest sensor have approximately equivalent processor resource requirements. The Data Distribution function of Figure IV.6 will provide MSDF with sensor data according to the selected central-level MHT fusion design. The detailed design of the MSDF function using MHT should be a subject of a separate study. In this study the scanning method for the central-level MHT fusion is selected. The performance of this approach is expected to be slightly lower than the approach where the sensor buffers are fused as they arrive, however, for the purpose of evaluating the processing requirements it is more organized in space and the performance parameters are easier to establish. Within this approach, the observation space is divided into sectors, the MSDF function scans sectors in sequence and fuses all contact data available within that sector.

The LRR, MRR and IRST sensors fused in the MSDF function are surveillance sensors using a TWS mode of operation. The scan period of the MSDF function is taken to be 0.25 seconds, and the azimuth horizon is taken to be divided into 32. Such TWS parameters impose that the processor run the entire set of algorithms within less than 1/128 seconds. The value of the MSDF scan period is based on the fact that since the MSDF and the sensors will not necessarily be in phase, it is preferable that MSDF scans at a period equal to the half of the lowest sensor scanning period (i.e., half of the IRST or the MRR scan period of 0.5 seconds). The number of sectors for a radar is normally related to the beam width and to computer storage consideration. Modern surveillance radars use 64 or 128 sectors, but since MSDF is not physically a sensor, it is not restricted to that choice. For the moment the value "32" suggested is tentative.

The sector division of the observational area means that the number of tracks and new contacts per sector must be 1/32 of the overall MSDF limit. The maximum number of contacts per sector that the MSDF must process is determined by the maximum number of contacts from each sensor of the AAW frigate. Based on sensor descriptions in Task I and the actual CPF radar, the LRR could process 1024 contacts per scan of 6 seconds, and the MRR and the IRST could process 128 contacts per

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scan of 0.5 second. Therefore, in 0.25 seconds, the MSDF should be able to process 1024/24 + (128+128)/2 = 171 contacts, which is the averaged contribution of each sensor over one MSDF scan. Considering the other sensors, a number of 256 contacts per scan as part of the benchmark algorithms is a safe choice. Reported on sector basis this means that the TWS operation will have to process up to eight new contacts per sector.

The number of tracks which will be maintained by the output management function and internally processed in the data association process will be set as equal to and twice the value of the number of contacts per scan. Thus $NT_2 = 256$ and $NT_1 = 512$ tracks per scan. As in surveillance radar, the TWS operation imposes that these two numbers be uniformly distributed over the sectors. So for each sector the benchmark algorithm must be capable of processing 16 tracks and retaining eight tracks for the database.

For the number of hypotheses and clusters the limits cannot be conditional to the sector. Instead the limits are based on the total observation area. Human factors considerations suggest (see Task V document) that M_2, the number of hypotheses retained by the MSDF function, can hardly be more than eight per cluster. For M_1 the internal process of association however must process many more. Thirty-two per cluster will be tentatively set. The number of clusters however, is not limited, but since it cannot be larger than the number of tracks (situation where all the targets are far apart) it is restricted to 256. Table IV.5 regroups all the limits and particularities of the benchmark MSDF function.

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Table IV.5. Limits and Particularities of the Benchmark MSDF Function

MSDF Limits and Particularities	Descriptions or values	
	Per Sector	Per MSDF Scan
Mode of Operation	Track-While-Scan	
Association Process	Multiple Hypothesis Tracking	
State Estimation Process	Adaptive Linear Kalman Filter	
Identity Estimation Process	Dempster-Shafer Reasoning	
Scan Period	0.25 Second	
Number of Sector	32	
Number of New Contact	8	256
Number of Retained tracks	8	256
Number of Processed tracks	16	512
Number of Retained Hypothesis	N.A.	8 (Per Cluster)
Number of Processed Hypothesis	N.A.	32 (Per Cluster)
Number of Clusters	up to 8	up to 256

IV.5.1 Benchmark Algorithms within Single General Purpose Processor

Figure IV.9 shows an information flow chart which represents the processing throughput of a single general purpose processor running the benchmark MSDF function of Figure IV.6 with limits and particularities of Table IV.5.

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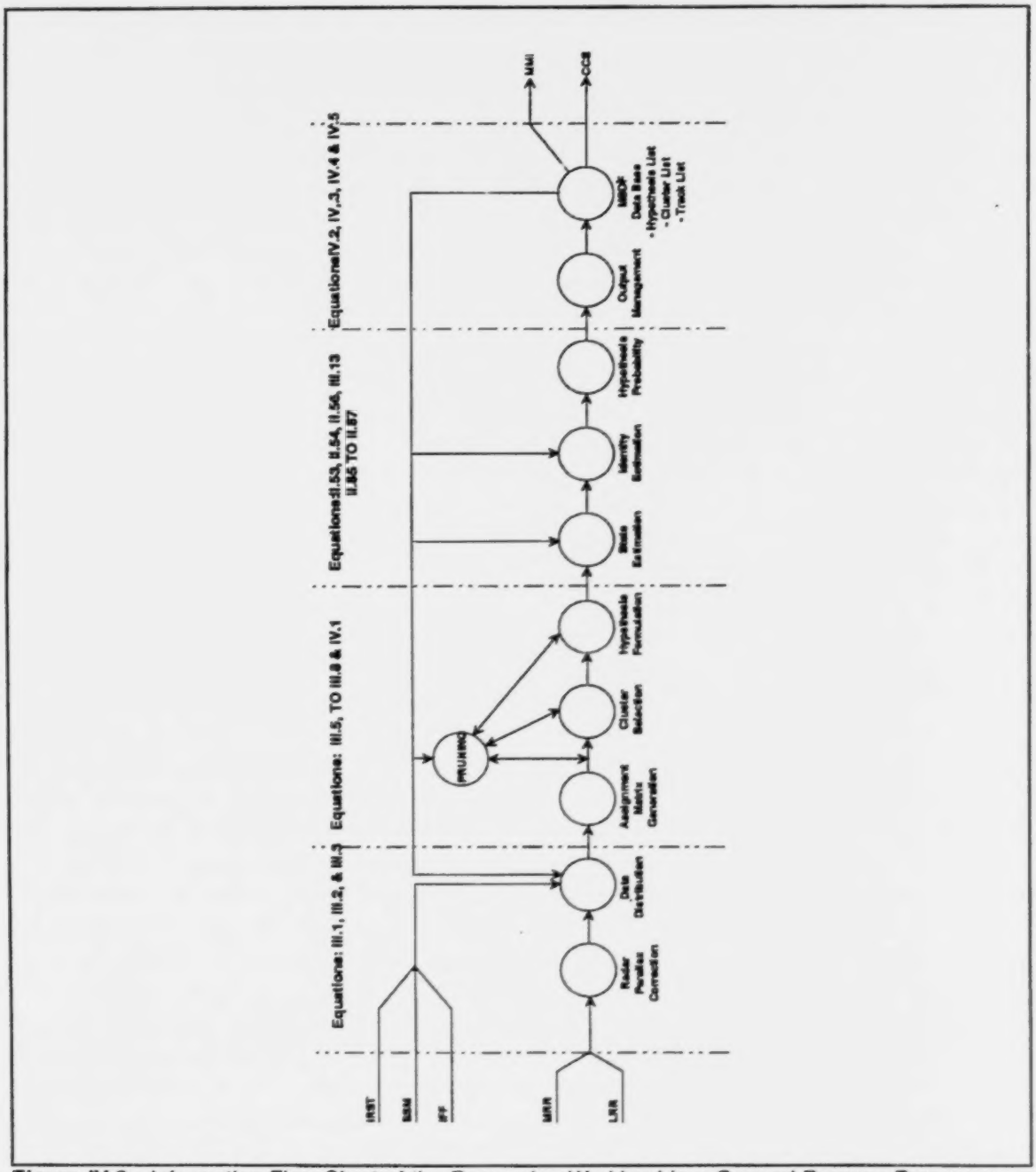

Figure IV.9 Information Flow Chart of the Processing Workload in a General Purpose Processor

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The selected processor is the AN/UYK-507 CB. The dashed lines separating the algorithms of the function are for clarity only and do not constrain or limit the implementation of the MSDF function beyond indicating where the main equations are performed.

In Appendix A the number of operations and the time required to perform each group of equations are explained and calculated. Table IV.6 regroups the results of the estimation of the processing required by the benchmark algorithms to be run on the actual AN/UYK-507. Since this is not a precise evaluation, to be on the conservative side, the most complex tactical situation was retained in the calculation.

Table IV.6. Estimated Processing Requirements of the General Purpose Processor

Functions	Main computer type of data operation	Estimated Processing Time per sector	Comments
Radar Parallax Correction	Floating Point	0.06 ms X 8 = 0.5 ms	Assume most unfavourable case (8 MRR contacts).
Data Distribution	Logical and Integer	Between 0.5 ms and 2 ms	Estimation based on actual CPF radar.
Assignment Matrix Generation	Floating Point	0.28 ms X 8 X 8 = 18 ms	Assume most unfavourable case (8 MRR contacts gated with 8 MSDF tracks).
Cluster Selection	Logical and Integer	Between 2 ms and 5 ms	Estimation based on time requested to order 64 integers. Also includes the pruning function.
Hypothesis Formulation	Logical and Integer	Between 2 ms and 5 ms	Estimation based on time requested to order 64 integers. Also includes the pruning function.
Hypothesis and Track Pruning	Logical and Integer	Included in cluster selection and hypothesis formulation	
State Estimation	Floating Point	0.22 ms X 16 = 3.5 ms	Assume most unfavourable case (16 tracks are updated with MRR contacts).
Identity Estimation	Floating Point	Tentatively assumed as equal to 3.5 ms as for state estimation	Dependent of threat database size. Tentatively assumed to be equal to state estimation.
Hypothesis Probability	Floating Point	0.06 ms X 32 = 2 ms	Assume most unfavourable case (one cluster containing 32 hypotheses and 16 tracks).
Output Management	Floating Point	0.16 ms X 8 = 1.3 ms	Assume unfavourable case where 8 pairs of tracks, forming 32 hypotheses, were pairing and combining.

From the estimated processing time of each function the overall processing can be estimated (for a situation where all the eight tracks and eight contacts are within one cluster) to be between 33 and 45 ms. The limits and particularities of the TWS mode described in Table IV.5 require that all the processing on one sector be performed within 7.8 ms.

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It is clear that this single general purpose processor architecture does not meet the processing requirement. The AN/UYK-507 (see appendix A) would have to be six times faster to process in real time the benchmark algorithms (without considering memory size limitation). In addition to the speed requirement there is the memory size required by the algorithms which is lacking in the AN/UYK-507. This processor has 256 Kbits RAM which would necessitate time consuming processes like swapping and using external memory.

IV.5.2 Benchmark Algorithms within a Parallel or Concurrent Processor

Figure IV.10 shows the information flow chart of the processing workload performed by a parallel or concurrent processor, running the benchmark data fusion function of Figure IV.6 with the characteristics of the Table IV.5. The proposed hardware device which can perform such computer processing is the AN/UYK-507/VME. The multiple processor architecture of this computer has 16 processors. There are various ways the processors can be connected. In this implementation one is used as master processor (CP) and 15 as co-processors (CoPs). The one shown in Figure IV.10 is selected because it ensures high performance. In the figure the vertical lines separate the chart to emphasise the algorithms which reside within the different processors.

The function which is the most time consuming, the assignment matrix generation, is performed by three independent processors. This divides the processing by a factor of 3. When many clusters must be generated and processed, three groups of three processors are available to perform the tasks of hypotheses formulation and evaluation. For example, CoP_5 gets the data of the second cluster and formulates the hypothesis. The tracks are then sent to the CoP_9 processor for state estimation and to the CoP_{10} for attribute estimation. The first co-processor that terminates processing, either CoP_9 or CoP_{10}, will have to compute the probability of all the hypotheses of the second cluster.

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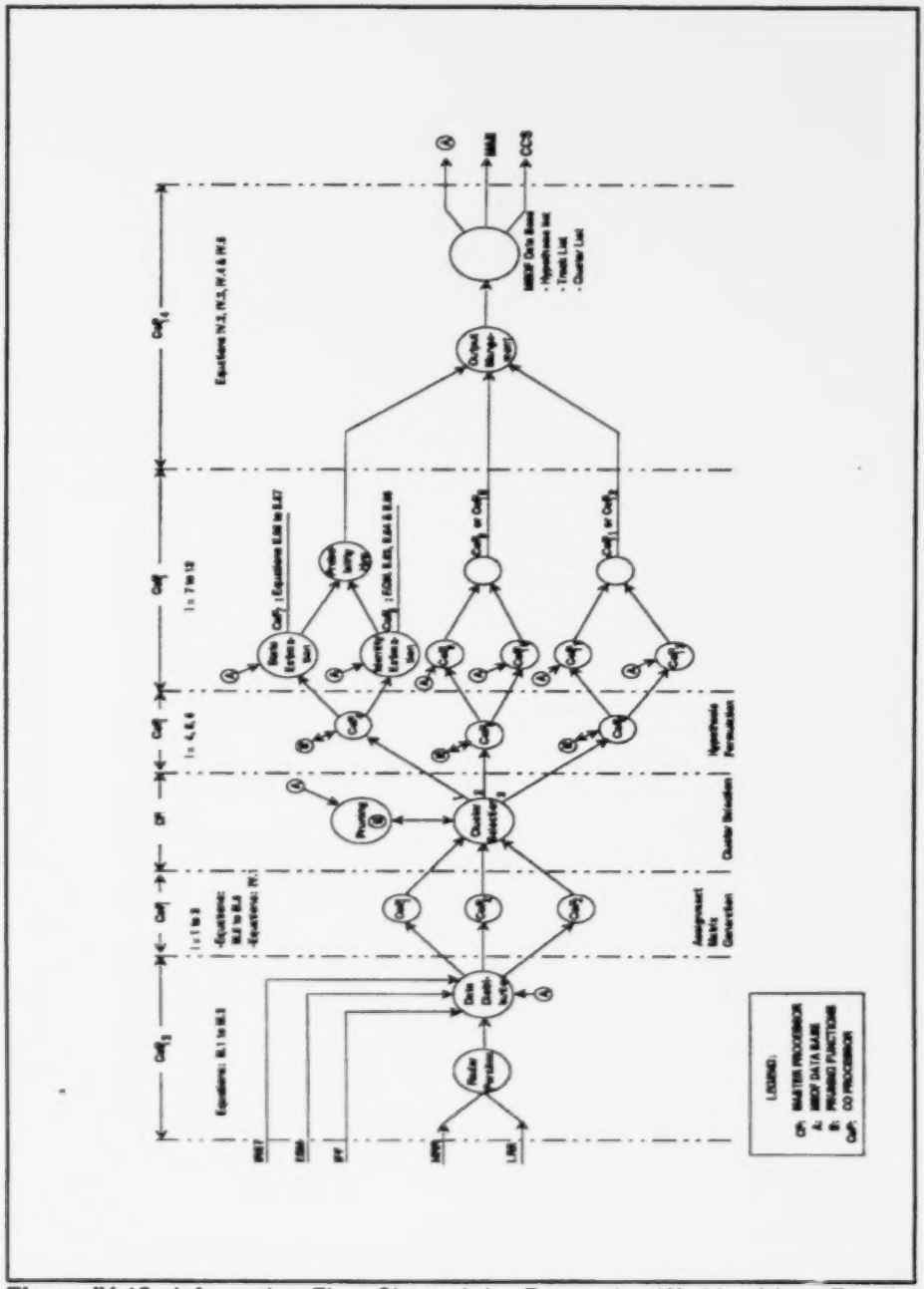

Figure IV.10 Information Flow Chart of the Processing Workload in a Parallel Processor

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Table IV.7 shows the estimated processing time required to run each function on the AN/UYK-507/VME. Appendix A presents the estimation process. The same assumptions as in single general purpose processor analysis were used.

Table IV.7. Estimated Processing Requirements for the Parallel Processing Computer

Functions	Estimated Processing Time per sector
Radar Parallax Correction	0.04 ms X 8 = 0.3 ms
Data Distribution	Between 0.5 ms and 2 ms
Assignment Matrix Generation	0.16 ms X 8 X 8 = 10 ms
Cluster Selection	Between 2 ms and 4 ms
Hypothesis Formulation	Between 2 ms and 4 ms
Hypothesis and Track Pruning	Included in cluster selection and hypothesis formulation
State Estimation	0.12 ms X 16 = 2 ms
Identity Estimation	Tentatively assumed as equal to 2 ms as for state estimation
Hypothesis Probability	0.04 ms X 32 = 1.3 ms
Output Management	0.09 ms X 8 = .7 ms

To estimate the total processing time, the parallelism between processors has to be taken into account. The vertical lines appearing in Figure IV.10 indicate into which processor the data goes as the sectors enter the TWS. After the initialization is performed, the data of sector "s" enters CoP_{13} where the alignment and TWS management functions are performed. As indicated in Table IV.7, this process can last up to 0.3+2 = 2.3 ms, which is less than the allocated maximum of 7.8 ms. After 7.8 ms the data from the "s+1" sector enters CoP_{13}, and the data of sector "s" is distributed in CoP_1 to CoP_3 for the function of track propagation and assignment matrix generation. Since these three processors work in parallel, it takes 10/3 ms to perform the task. After another 7.8 ms, the data from sector "s+2" enters CoP_{13}, sector "s+1" is already inside CoP_1 to CoP_3 and sector "s" data is inside the master CP where the cluster selection is performed. This task is estimated to last less than 4 ms, which is under the limit of 7.8 ms. Another step later, sector "s" data enters the three processors allocated for hypothesis formulation of each cluster, CoP_4 to CoP_6, while fourth sector data, that of sector "s+3", has entered the process. The formulation of the hypothesis is also estimated to take 4

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ms in the most complicated case where the 16 tracks and the eight contacts are all located in a single cluster. When more clusters are involved, the formulated hypotheses are less complicated and less demanding of processing time due to the relatively small number of data inside each cluster. In the extreme situation where 16 clusters exist the hypothesis formulation is straightforward and takes less than 0.5 ms for each cluster. When three coprocessors share the work in parallel, a maximum of 3 ms is necessary for the accomplishment of the task. Another 7.8 ms later, all the tracks (a maximum of 16), generated and existing in a set of hypotheses are sent to the state estimation and identity estimation process in the CoP_{2i-1} and CoP_{2i} processors respectively (i=4,5,6). In the extreme situation, this task should last 2 ms for the state estimation. The identity estimation is more complicated to evaluate since the precise mathematical structure of a Dempster-Shafer algorithm for identity estimation purposes is still under research and development and the size of the threat database is unknown. From PARAMAX experience on CPF in the area of EW, it is realistic to assume that a time in the same order as state estimation is possible for this task. Whatever the exact value, this is definitely lower than the maximum 7.8 ms. When one of the processors has finished the estimation it takes charge of the hypotheses probability calculation, process of no more than 1.3 ms. The resulting duration is therefore 3.3 ms for these three computations. Three pairs of processors are used to perform these computations because there can be many clusters. In case there are more than six clusters three pairs of coprocessors may not appear to be sufficient since the work lasts 3.3 ms. But clustering (and also the functional limits stated in Table IV.5) has the advantage of reducing the density of data per cluster, which results in faster hypothesis formulation and evaluation due to a relatively lower number of tracks and contacts per cluster. When the processed data of sector "s" reaches the last step in processor CoP_{14}, the data of sector "s+5" has entered the introductory function of alignment. CoP_{14} is responsible for the task of output management, which includes combining and pruning excess hypothesis and tracks and the task of preparing the results of the MSDF database for MMI, CCS and broadcast to other processors. This task is relatively brief and done quickly. The output management processing time is estimated to be 0.7 ms. The MSDF database work must be added since the database operation is executed in the same processor. Compared to CPF similar functions this work will probably last approximately 2 ms.

Table IV.8 below lists the estimated processing time for each step of the TWS process. All the times are lower than the limit of 7.8 ms but this is not enough to ensure the functionality of all the benchmark algorithms. The proposed AN/UYK-507/VME has only one bus to transfer data among the 16 processors. The transfer rate is 10 mega floating points (32 bits) data per second. Thus this transfer of data will add a certain time to each step. This extra time is hard to evaluate but a first approximation can be made. Among all the processors, CoP_4 to CoP_8 have to transfer the largest amount of data to the state estimation processor. In the worst case this can be a list of 16 tracks and eight contacts. This represents no more than 1024 floating point words (32 bits). To transfer this

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batch of data the VME bus will require 0.1 ms. The most unfavourable case is when the 16 processors have to communicate the same amount of data at the same moment. Since only one amount is transferable it may take 1.6 ms to complete the 16 transfers. An additional 50 % of this time is included to take into account the overhead and other processing considerations. Therefore, 2.5 ms must be added to each step. With this additional of time, the processors are still under the 7.8 ms limit.

Table IV.8. Processing Estimates for each Step of TWS Process

Step	Estimated Processing time
1	2.3 ms
2	3.3 ms
3	4 ms
4	4 ms
5	3.3 ms
6	2.7 ms

When the last steps have been performed the data of sector "s" is approximately 6X7.8 = 47 ms old which is highly acceptable. And unlike the single general purpose processor, the TWS tracker does not accumulate retardation since the sector data enters and exits the MSDF function within the sector scan period. In conclusion, the proposed AN/UYK-507/VME seems to be capable of running the benchmark algorithms.

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IV.6 Concluding Remarks

This report discussed the possible computer architectures and the general performances of the AN/UYK-507 computer. This study has shown that the existing AN/UYK-507 CB computer can use only one CoP, thus limiting the performance of the MSDF algorithms discussed in the Task III report. The AN/UYK-507 CB could perform approximately 10 MIPS with the CoP added to the CB working along with the CP and performing parallel processing. This actual architecture could be a short term solution for sensor-level fusion for MSDF processing.

As the technology advances, threats will become quicker and harder to detect, and the performance of the sensor-level architecture may not be satisfactory to encounter these threats. With technology advancements, sensors will become more sophisticated, additional sensors will be included in the MSDF process and more complex fusion architectures (e.g., central level) could be required to detect and identify threats of the year 2000 and beyond. Such systems impose much higher requirements for processor resources. In order to respond to this demand, the 507 VME architecture has been proposed. It was estimated that the AN/UYK-507 VME computer can perform about 100 MIPS. The software within this computer can be designed to use the parallel processing capability of the computer in many ways. This report has proposed a way to parallelize the central level fusion algorithms, which ensures processing of sensor contact data from all sensors of the AAW Frigate described in Task I, in a track-while-scan mode, within a central level fusion architecture.

The AN/UYK-507 VME computer is deemed able to satisfy the MSDF demand of the years 2000 for central level fusion. The next phase should be prototype implementations, which will evaluate and optimize the method of parallelizing the software implementation and perform quantitative measurement of the performance of the central level fusion for the AAW frigate.

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APPENDIX IV-A

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APPENDIX A - Evaluation of the Computer Processing Time

This appendix shows how to estimate the number of mathematical operations required to perform some tasks of the MSDF function described in the Task IV report. The equations presented can be found in the Task II, III and IV reports for the implementation of Central Level Fusion. In the starting chapter, the processing time necessary to process the MSDF equations is estimated and explained in detail for the AN/UYK-507 Common Bus (CB) computer described in section IV.2. The second chapter discuss the case of the AN/UYK-507 VME which is described in section IV.3. From the computer AN/UYK-507 assembly language, it is possible to find the approximate number of instructions for each set of equations performing the prescribed functions. This should give a rough approximation of the number of instructions performed by the AN/UYK-507 CB and the AN/UYK-507 VME.

A.1 CPU Time for the AN/UYK-507 CB Computer

The mathematical operations, the CPU cycle/operation and the instruction time with memory reference in cache are given in Table A.1. The last column indicates how much supplementary time must be added when the operation request external memory reference is not cached. There are 16 kinds of mathematical operations which are considered in this table and three may use the external memory, the load, the store and the equal operation. The CPU clock speed is 45 MHz, with a CPU cycle time of approximately 89 ns. All operations are considered floating point operations. The external memory reference time is 13 CPU cycles or 579 ns. Memory reference is not always time necessary for the three operations. A safe evaluation [Lecuyer and Bourassa, 1992] suggests that it could be necessary 10% of time. From the data in Table A.1 the total CPU time to execute a given set of equations, TCPTIME, is calculated as follows:

$$TCPTIME = \sum_{i=1}^{16} NUMOP(i) \times CPUTIME(i) + MEMREFS \times (1 - CACHEHIT) \times 579ns \quad \text{(A.1)}$$

where TCPTIME is the total AN/UYK-507 CB CPU time to process the equation, NUMOP(i) is the number of operations of the mathematical operation "i", CPUTIME(i) is the single CPU time for the mathematical operation "i", MEMREFS is the total number of memory references when not cached, and CACHEHIT is the access ratio to the cache memory (90%). With this equation it is therefore possible to calculate the total AN/UYK-507 CB CPU time at 90% cachehit rate for each set of equations for Central Level Fusion Algorithms. The following sections present the application of equation A.1 for each MSDF benchmark algorithm requiring mathematical equations.

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Table IV.A1. Number of Operations for Equations

MATH OPERATIONS	CPU CYCLE/OPERATION	INSTRUCTION TIME (ns); MEM REF IN CACHE	INSTRUCTION TIME (ns); MEM REF NOT CACHED
Add	2	178	N.A.
Subtract	2	178	N.A.
Multiply	2	178	N.A.
Divide	4	356	N.A.
Square[1]	2	178	N.A.
Square Root	42	3738	N.A.
Equal[2]	1	89	579
Store	1	89	579
Load	1	89	579
Cos x	98	8722	N.A.
Sin x	98	8722	N.A.
Arctan x	84	7476	N.A.
Change sign	1	89	N.A.
Exponential e^x	95	8455	N.A.
Natural Log ln x	93	8277	N.A.
Exponent[3] $y = a^x$	190	16910	N.A.

Note[1]: Same as Multiply

Note[2]: Same as Store

Note[3]: Exponent function is a complex set of instructions

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A.1.1 Radar Parallax Correction

The equations involved in the parallax correction are the following:

$$r = [r'^2 + \Delta r^2 + 2r'(\Delta x \sin\beta' \cos\theta' + \Delta y \cos\beta' \cos\theta' + \Delta z \sin\theta')]^{1/2} \quad \text{(A.2)}$$

$$\beta = \arctan\left[\frac{r' \sin\beta' \cos\theta' + \Delta x}{r' \cos\beta' \cos\theta' + \Delta y}\right] \quad \text{(A.3)}$$

$$\theta = \arctan\left[\frac{r' \sin\theta' + \Delta z}{[r'^2 \cos^2\theta' + \Delta x^2 + \Delta y^2 + cte]^{1/2}}\right] \quad \text{(A.4)}$$

$$cte = 2r' \cos\theta' (\Delta x \sin\beta' + \Delta y \cos\beta')$$
$$\Delta r^2 = \Delta x^2 + \Delta y^2 + \Delta z^2 \quad \text{(A.5)}$$

To calculate total CPU time for this set of equations, the coding of the algorithm was assumed done in such a way as to minimize the number of mathematical operations, taking into account that some calculations are repeated and do not have to be recomputed by the processor, e.g., the computation of cosβ' which appears three times. Furthermore concerning the initial constant value it was assumed that it is preferable to save Δr^2 instead of Δr. Table A.2 outlines the mathematical operation of the radar parallax correction.

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Table IV.A2. Radar Parallax Correction Estimation

MATH OPERATIONS	TOTAL INSTRUCTIONS	TOTAL INSTRUCTION TIME (ns) MEM REF IN CACHE	INSTRUCTION TIME (ns); MEM REF NOT CACHED (OPE. x 579 ns)
Add	11	1958	0
Subtract	0	0	0
Multiply	8	1424	0
Divide	2	712	0
Square	0	0	0
Square Root	2	7476	0
Equal	3	267	1737
Store	30	2670	17370
Load	54	4806	31266
Cos x	2	17444	0
Sin x	2	17444	0
Arctan x	0	0	0
Change sign	0	0	0
Exponential e^x	0	0	0
Natural Log ln x	0	0	0
Exponent $y = a^x$	0	0	0
TOTAL	114	54201	50373

From equation A.1 the total processing time is given as:

TCPTIME = 0.054201 ms + 0.050373 X 10% ms = 0.059 ms

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A.1.2 Track Propagation and Gating

The equations involved in track propagation and gating are the following:

$$\vec{X}(j\,|\,k) = \Phi(t_j - t_k)\vec{X}(k|k) \tag{A.6}$$

$$P(j|k) = \Phi(t_j - t_k)\,P(k|k)\Phi^T(t_j - t_k) + Q \tag{A.7}$$

$$d_{ij}^2(k) = \left[\vec{Y}_i(k) - H\vec{X}_j(k\,|\,k-1)\right]\left[U_{ij}(k)\right]^{-1}\left[\vec{Y}_i(k) - H\vec{X}_j(k\,|\,k-1)\right]^T \tag{A.8}$$

$$U_{ij}(k) = R_i(k) + H P_j(k\,|\,k-1)H^T \tag{A.9}$$

$$C_{ij} = 2\ln\left[\frac{P_D}{(1-P_D)\sqrt{(2\pi)^{M_z}\beta_{fa}V_{ij}\det(U_{ij})}}\right] - d_{ij}^2 + 2\ln\left[\frac{P(Z_i\,|\,\hat{Z}_j)}{P(Z_i\,|\,NewTarget)}\right] \tag{A.10}$$

These equations contain some redundancy. The evaluation of the inverse of the matrix U appearing in equation A.8 necessitate a lot of manipulation, some of which is useful in other equations. To inverse the matrix U its determinant must be evaluated. Therefore, this operation does not have to be recomputed in equation A.10. Table A.3 outlines the mathematical operation of track propagation and gating function.

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Table IV.A3. Track Propagation and Gating Estimation

MATH OPERATIONS	TOTAL INSTRUCTIONS	TOTAL INSTRUCTION TIME (ns) MEM REF IN CACHE	INSTRUCTION TIME (ns); MEM REF NOT CACHED (OPE. x 579 ns)
Add	171	30438	0
Subtract	6	1068	0
Multiply	153	27234	0
Divide	12	4272	0
Square	0	0	0
Square Root	1	3738	0
Equal	64	5696	37056
Store	448	39872	259392
Load	854	76006	494466
Cos x	0	0	0
Sin x	0	0	0
Arctan x	0	0	0
Change sign	40	3560	0
Exponential e^x	0	0	0
Natural Log ln x	1	8277	0
Exponent $y = a^x$	0	0	0
TOTAL	1750	200161	790914

From equation A.1 the total processing time is given as:

TCPTIME = 0.200161 ms + 0.0790914 X 10% ms = 0.279 ms

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A.1.3 Probability Evaluation

The following equation is used for hypothesis probability evaluation.

$$Pr(k) = Pr(k-1)\left(\frac{1}{C}\right)(P_D)^{N_a}(1-P_D)^{N_t-N_a}(Bff)^{N_f}(Bkf)^{N_k}\prod_{j=1}^{N_a}\frac{\exp\left\{-\frac{\vec{Z}_j(k)^T S_j(k|k-1)^{-1}\vec{Z}_j(k)}{2}\right\}}{\sqrt{(2\pi)^{dim(S)}\det(S)}} \quad \text{(A.11)}$$

$$\vec{Z}_j = \vec{Y}_j(k) - H_j(k)\,\hat{\vec{X}}_j(k|k-1)$$

This equation has many terms which are computed in the track propagation and gating section. For example, the matrix S(k|k-1) in the exponential function is exactly the same as the matrix U in the previous section. The program will not recompute these terms but will simply receive the already completed values. This was considered in the estimation of the number of operations. Also, to save processing time it is recommended that the product of exponential function be changed by an exponential of a sum. This too was considered in the estimation of the number of operations in Table A.4.

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Table IV.A4. Probability Evaluation Estimation

MATH OPERATIONS	TOTAL INSTRUCTIONS	TOTAL INSTRUCTION TIME (ns) MEM REF IN CACHE	INSTRUCTION TIME (ns); MEM REF NOT CACHED (OPE. x 579 ns)
Add	15	26708	0
Subtract	2	356	0
Multiply	53	9434	0
Divide	3	1068	0
Square	0	0	0
Square Root	1	3738	0
Equal	1	89	579
Store	80	7120	4630
Load	148	13172	85692
Cos x	0	0	0
Sin x	0	0	0
Arctan x	0	0	0
Change sign	0	0	0
Exponential e^x	1	5455	0
Natural Log ln x	0	0	0
Exponent $y = a^x$	0	0	0
TOTAL	304	46102	132591

From equation A.1 the total processing time is given as:

TCPTIME = 0.046102 ms + 0.132591 X 10% ms = 0.059 ms

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A.1.4 Combining Track

The output management process comprises the combining tracks formulas given below.

$$|x_{ai} - x_{bi}| \leq \beta\sqrt{\sigma_{ai}^2 + \sigma_{bi}^2} \tag{A.12}$$

$$\gamma^{-1} \leq \frac{\sigma_{ai}^2}{\sigma_{bi}^2} \leq \gamma \tag{A.13}$$

$$\vec{X} = \frac{Pr(a)\vec{X}_a + Pr(b)\vec{X}_b}{Pr(a) + Pr(b)} \tag{A.14}$$

$$P = \frac{Pr(a)P_a + Pr(b)P_b}{Pr(a) + Pr(b)} + \frac{Pr(a)Pr(b)}{[Pr(a) + Pr(b)]^2}(\vec{X}_a - \vec{X}_b)(\vec{X}_a - \vec{X}_b)^T \tag{A.15}$$

Table A.5 outlines the mathematical operation to combine tracks.

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Table IV.A5. Combining Tracks Estimation

MATH OPERATIONS	TOTAL INSTRUCTIONS	TOTAL INSTRUCTION TIME (ns) MEM REF IN CACHE	INSTRUCTION TIME (ns); MEM REF NOT CACHED (OPE. x 579 ns)
Add	47	8366	0
Subtract	6	534	0
Multiply	134	23852	0
Divide	9	3204	0
Square	0	0	0
Square Root	0	0	0
Equal	60	5340	34740
Store	256	22784	148224
Load	512	45568	296448
Cos x	0	0	0
Sin x	0	0	0
Arctan x	0	0	0
Change sign	0	0	0
Exponential e^x	0	0	0
Natural Log ln x	0	0	0
Exponent $y = a^x$	0	0	0
TOTAL	1024	109648	479412

From equation A.1 the total processing time is given as:

TCPTIME = 0.109648 ms + 0.479412 X 10% ms = 0.158 ms

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A.1.5 Measurement Update of the Kalman Filter

The state estimation process performed the measurement update of the Kalman filter using these following equations:

$$K(k+1) = \Phi(k+1)P(k+1|k)H^T(k+1)S^{-1}(k+1) \quad \text{(A.16)}$$

$$\hat{X}(k+1 \mid k+1) = \hat{X}(k+1 \mid k) + K(k+1)Z^{\wedge}(k+1 \mid k) \quad \text{(A.17)}$$

$$P(k+1 \mid k+1) = [I - K(k+1)H(k+1)]P(k+1 \mid k) \quad \text{(A.18)}$$

The matrix S appearing in equation A.16 has already been inverted in equation A.3 of the track propagation and gating function (where it is named U). Therefore the value was assumed saved and passed on to the state estimation process. The same supposition is applied to the residual vector Z which is also computed in equation A.3. Table A.6 outlines the mathematical operation for the measurement update of the Kalman filter.

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Table IV.A6. Measurement Update of the Kalman Filter Estimation

MATH OPERATIONS	TOTAL INSTRUCTIONS	TOTAL INSTRUCTION TIME (ns) MEM REF IN CACHE	INSTRUCTION TIME (ns); MEM REF NOT CACHED (OPE. x 579 ns)
Add	129	22962	0
Subtract	0	0	0
Multiply	162	28836	0
Divide	0	0	0
Square	0	0	0
Square Root	0	0	0
Equal	60	5340	34740
Store	351	31239	203229
Load	702	62478	406458
Cos x	0	0	0
Sin x	0	0	0
Arctan x	0	0	0
Change sign	0	0	0
Exponential e^x	0	0	0
Natural Log ln x	0	0	0
Exponent $y = a^x$	0	0	0
TOTAL	1404	150855	644427

From equation A.1 the total processing time is given as:

TCPTIME = 0.150855 ms + 0.644427 X 10% ms = 0.215 ms

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A.2 CPU Time for the AN/UYK-507 VME Computer

For the future AN/UYK-507 VME computer, the total instruction CPU time memory referenced in cache was decreased by 20% since the clock will be increased by approximately 20%. Therefore all the data in the third column of tables A.2 to A.6 is multiplied by 80%. Also it is assumed that memory referenced "not cached" will not be used because of the increase in cache memory and the use of local memory on each central processor and coprocessor card of the AN/UYK-507 VME computer. Therefore the total CPU time (TCPTIME) for the AN/UYK-507 VME computer is obtained by cancelling the last term in equation A.1 and multiplying the first term by 80%.

Table A.7 below regroups all the processing time for each MSDF function treated in sections A.1.1 to A.1.5 and for each computer.

Table IV.A7. Estimated CPU Time for the AN/UYK-507 CB and VME Computers

SECTION	Total CPU Time (ms)	
	AN/UYK-507 CB	AN/UYK-507 VME
A.1.1	0.059	0.043
A.1.2	0.279	0.160
A.1.3	0.059	0.037
A.1.4	0.158	0.089
A.1.5	0.215	0.121

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TASK V - Study of Displays and Man-Machine Interface

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Task V: Study of Displays and Man-Machine Interface

The objective of this contract is to undertake a study of Multiple Sensor Data Fusion (MSDF) techniques and issues, to analyze, evaluate and propose data fusion algorithms integrating data acquired from dissimilar sensors within the same platform, to study and select the Hardware/Software environment supporting these algorithms, to propose Research and Development topics related to the MSDF domain based on the above analysis, and to analyze the feasibility of implementing an MSDF function within the operational land-based test facility - Combat System Test and Support Facility (CSTSF) at PARAMAX.

This study is the fifth analysis, to be delivered with the fourth analysis, of the six reports performed to accomplish the objective of this contract. Based on the studies found in the course of the Literature Survey, which focus upon or include a discussion of operator-machine (or man-machine) interface (OMI or MMI) issues, this analysis will document and discuss the OMI aspects of MSDF processes and architectures addressed in Tasks II and III for the AAW Frigate described in Task I of this project.

The MMI study consists of the following:

1. Literature Survey
2. Man-Machine Interface Issues on the AAW Frigate.

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V.1 Literature Survey

Data fusion algorithms, and multiple hypotheses tracking algorithms in particular should reduce the workload of the operator to allow him/her to concentrate on the significance of the information being collected rather than on the details of the collection of this information. But without a thorough consideration of the way the information is made available to the operator, these algorithms may be worthless and may even add to the operator's workload. Hence the design of the OMI should receive careful attention.

A brief literature survey was performed on subjects which discuss the relation between the data fusion and the operator interface. The search was conducted for literature concerning three main topics:

1. Operator requirements for an AAW data fusion function
2. Operator requirements and the multiple hypothesis tracking method
3. Operator requirements and database management.

Only a dozen papers were found which discussed these subjects to any extent. This small number can be explained by the criteria of fusion closeness, an important discriminator. Papers addressing the same subject but within the ASW context were considered when their conclusions could be extended to the AAW context. The IEEE Transactions on Systems, Man and Cybernetics, among the regularly published journals, was found to be the best source of articles on OMIs in detection and tracking systems in general and on the fusion of information from different sensors. For example, a recent issue of this journal (volume 21, Number 5, September/October 1991) had a special section on Distributed Sensor Networks. Proceedings from various specialized symposia and conferences on Data Fusion also included some pertinent presentations on OMI issues. Some of the articles found pertinent to this analysis are discussed below.

The article by [Schwartz, Kullback and Shrier, 1986] presents a framework for designing systems involving task cooperation between intelligent components and gives as a specific example of the integration of human-computer interaction in the solution of fusion problems. It stresses the need to evaluate the strengths and weaknesses of both the human and the computer in order to optimize human-machine interaction. For example, humans tend to evaluate some of the uncertainties subjectively, overestimating the process noise (enemy behaviour) and underestimating the measurements noise (sensor error) so that the correlation portion of the fusion is better performed by the computer. On the other hand, humans are superior at establishing data relevance and integrating sensor data with military doctrine.

[Everett, 1990] while describing the operator interaction in a prototype of the multiple-hypothesis

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tracker of an Advanced Data Fusion System for surface ship surveillance is more specific about the actions performed by the operator. These actions must allow the operator to correct inevitable miscorrelations inherent to "automatic correlation". These operations (e.g., deleting or adding a report to a track, merging or splitting tracks) are performed for the "top" hypotheses (hypotheses with the highest probability) but have repercussions on the lower hypotheses; hence there should be a means for these actions to be undone since they can produce inconsistent or unexpected results.

[Bottlik and Blackman, 1989] argue that it is desirable to present to the operator more than just the "best" hypothesis, and they develop a "coordinated presentation" which abstracts pertinent information from all the significant hypotheses. This coordinated presentation involves assigning a single estimator for the number of tracks in the system instead of a set of track probabilities as an indicator of the state of the system. But the typical case they use to illustrate their approach is depicting position only and they recognize that to extend their approach to two or three dimensional coordinate systems would mean loss of time history display and that further study is needed for implementation.

V.2 Man-Machine Interface Issues on the AAW Frigate

In the course of the literature survey, PARAMAX has identified few reports and articles which focus upon, or include a discussion of, OMI issues which are specific and exclusive to an AAW MSDF function. Some documents prepared for various U.S. Navy agencies (NOSC, SPAWAR, etc.) were found to share similar objectives with this task. They address certain points and propose some design implementations which can be applied for the purpose of this task. However there is a unique characteristic to an MSDF function which uses multiple hypothesis tracking method for data association. With MHT the operator of the MSDF function has the possibility of getting more than one tactical display due to the various hypotheses which can be generated. The articles which discuss this characteristic, address the correlation accuracy aspect of their propositions and do not particularly address the human factor aspect of their propositions.

Before designing an OMI the engineers and the ergonomic scientists had to identify in detail the duties to be assigned to each operator responsible for the function. This implies that all the particularities of the function which require or permit operator control or input must be also clearly identified. Due to the fact that the concept of data fusion (especially one using the MHT method) onboard a naval platform is relatively new, an accurate identification of those functionalities has not yet been delimited. However there is a tendency which can be observed in the OMI design documents of recently proposed C^2 systems [Kastella et all., 1992; NOSC, 1989; SPAWAR, 1989; SPAWAR 1990] concerning the presentation of data and results to the operator. In these documents a windowing environment based on the MIT developed X-WINDOW [Jones, 1988] is proposed. There is no

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mention of human engineering studies which support the choice of X-WINDOW. These kind of human engineering studies are highly context dependent. For the selection of the OMI content on the AAW frigate, scenarios within the real or prototype environment to measure the human reaction information are needed, instead of extrapolation from another context. For example a human engineering study performed in an ASW context on the management of multiple window sonar displays shows that only 10% of operator errors were due to the window monitoring [Matthews and McFadden, 1989]. The AAW MSDF function context of this Task V is so different from the ASW sonar situation that the application of the same conclusion is unrealistic.

In a near future the appropriate OMI engineering studies applicable to various AAW contexts will probably be performed. For the moment, the popularity of the X-WINDOW probably explains why the windowing environments are now the most often proposed approach in the new CCS or other systems. For the frigate of the year 2010 the windowing environment will certainly be used, but perhaps more advanced software packages or versions of X-WINDOW will be utilized and the human factor will be more circumscribed.

V.2.1 Integrated Real-Time Displays of MHT Results

The proposed MSDF benchmark algorithms of Task IV used the MHT method to associate the input contacts with the MSDF tracks. When the targets are closely spaced inside one cluster, the ambiguity leads to formation of many plausible tactical situations called hypotheses. When many hypotheses have to be presented, the operator can be totally overloaded with information and be unable to judge the situation or make a decision. Also an inadequate display format of the various tactical situations could lead to an undecodable picture.

The work performed by [Bottlik and Blackman, 1989] and [Everett, 1990] are the only studies found, which have addressed the adaptation of the MHT results and the operator capacity. The first paper discusses the way the hypotheses are presented while the second one discusses the management tasks, called actions, performed by the operator. These actions have an impact on the presentation of the hypotheses. The following sections outline the ideas presented in these two studies.

V.2.1.1 Interaction Between the Operator and the MHT Algorithm

Everett assumes that the operator has the possibility to interact with the MHT process by performing some specific data association actions. It is not the goal of this task to explain the details of each action in term of implementation, mathematics and processing. It is the operator aspect that is of concern in this report. These actions are listed in the following table:

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Table V.1. Action Performed by the Operator

Action	Undone Action	Consistency Checks
Deleting a report from the MSDF database	Request confirmation	No
Deleting a track from the MSDF database	Request confirmation	No
Removing a report from a track	Adding a report to a track	No
Adding a report to a track	Removing a report from a track	Yes
Initializing a track with an existing report	Adding a report to track	Yes
Merging tracks	Splitting tracks	Yes
Splitting tracks	Merging tracks	Yes

These actions are necessary to improve the quality of the fusion of the information but in an AAW context the situation changes rapidly. The context of the Everett work is ship surveillance, where the typical speed of the targets are in the order of 20 knots compared to 300 knots in AAW. In spite of this rapidly changing tactical situation environment PARAMAX believes that all the operators performing tracking and situation analysis should be able to interfere into the MHT process to reduce the ambiguity. Hence they should have the capability to apply the above actions. The actions shown in Table V.1 are presented with the correction processes to undo actions. The last column indicates if the action will be evaluated for consistency by the MHT algorithm. The consistency check makes sure that the actions performed by an operator do not violate some internal association rules specific to MHT where upon the action would be refused by the fusion function.

For implementation reasons, Everett did not consider the possibility of reversing the action of removing a report or a track from the data fusion function. The experience PARAMAX has gained with CPF shows that it is sometimes necessary to input reports or tracks manually into a system. Therefore it is suggested that two other operator actions, adding a report or a track to the MSDF database, be included in the actions listed in Table V.1.

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V.2.1.2 Displays of Multiple Hypothesis

The hypotheses generated by MHT for a specific cluster represents different tactical situations. Some could have many tracks in common and some may be completely disparate. From a statistician's point of view all hypotheses with non-vanishing probability have some importance and should be presented to the operator. For human factor considerations, the simultaneous presentation of eight hypotheses (the benchmark algorithm in Task IV suggests limiting the number of hypotheses to eight) could be cumbersome.

In the OMI algorithm of the PARAMAX (EISG Eagan, MN) ASW data fusion system, Anti Submarine Warfare Information Systems (ASWIS) [Kastella et all., 1992] gives many choices to the operator concerning the hypotheses. The operator can select as many hypotheses as he/she wants-the best, the best with the second best, the fourth best only, etc. Here the world "best" means the most probable. This particularity of the ASWIS OMI has been implemented for debugging and development considerations and not necessarily for human factor considerations. Such a prototype system for the AAW frigate would be the ideal tool to optimize the OMI in this context.

[Bottlik and Blackman, 1989] have evaluated and compared four display approaches: nearest neighbour display results, best hypothesis display best hypothesis with track probability display and a proposed one called coordinate presentation display.

The confusing situation of nearest neighbour in high target density is well known (see figure 5 of [Bottlik and Blackman, 1989]) and this approach is inappropriate for central-level fusion.

The display of the best hypothesis improves the quality of the presentation in the sense that the operator knows the probability of the hypothesis which is a measure of the state of ambiguity in the real tactical situation. In the situation where the probability of this best hypothesis is close to unity the presentation is instructive and close to the real situation. But when this is not the case and, in addition, two or more hypotheses have probability of the same order, the display of the best is no more instructive than the second, third or other best hypotheses.

An improvement in this situation will be the inclusion of the probability of each track which pertains to the best hypothesis (see figure 3 of [Bottlik and Blackman, 1989]). In MHT the probability of a track is not a used concept as it is in the probability of a hypothesis. Track probability is obtained from:

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$$p_t = \sum_{H:\, t \in H} p_H \qquad \text{(V.1)}$$

where the sum is over all the hypotheses which have the track. Showing this number with that track on the tactical display of the best hypothesis helps the operator to evaluate which tracks are the cause of ambiguity.

Still a problem persists with the best hypothesis with track probability display approach in situations of low hypothesis probability. In such situations the number of tracks can vary as time evolves. This variation is a natural phenomenon since the number of tracks in a hypothesis is a statistical random variable. But when the operator has not accessed or cannot have access to the other hypotheses, his/her interpretation of the tactical situation can be erroneous. To overcome this problem [Bottlik and Blackman, 1989] propose the coordinate presentation display.

In this display the operator sees objects which are conglomerates of tracks (see figure 4 of [Bottlik and Blackman, 1989]). The conglomerate objects are obtained from a track probability which is the averaging of the tracks which belong to the conglomerate. Mathematically, the state vector and the covariance matrix of a conglomerate of tracks are given by:

$$\vec{X}_c = \frac{\sum_{t \in C} p_t \vec{X}_t}{\sum_{t \in C} p_t} \qquad \text{(V.2)}$$

$$P_C = \frac{\sum_{t \in C} p_t \left(P_t + \vec{X}_t \vec{X}_t^T \right)}{\sum_{t \in C} p_t} - \vec{X}_C \vec{X}_C^T \qquad \text{(V.3)}$$

The mathematical formulation which permits the selection of a conglomerate track set is cumbersome. Geometrically, a track pertains to a conglomerate if this track has at least one contact in common with a least one other track of the conglomerate (see reference for mathematical expression). The statistical characteristic of a conglomerate of tracks is the number of "distinct" tracks which compose it. This number is obtained from the sum of the probability of each track pertaining to the conglomerate; the denominator term in equation V.2. This number is a continuous random variable and could be interpreted as the expected number of established targets in the conglomerate. The distinction between a conglomerate and a cluster is mathematically clear but geometrically they are similar objects. A cluster is a group of tracks connected by their gate while the tracks in a conglomerate are connected by common reports. A cluster can contain many conglomerates.

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According to the authors Bottlik and Blackman, the coordinated display method combines information from all the significant hypotheses to yield a compact presentation. The confusion and the ambiguity due to the high density of new targets is indicated through the number of "distinct" tracks. The advantage of this method is consistency because the tracks do not erratically appear and disappear and the poor tracks are presented in a simple and meaningful way.

Mathematically the formulation of the method is not yet complete. Aspects concerning the time evolution of the number of tracks in a conglomerate, especially that related to when conglomerates split or merge, need to be clarified. One of the authors has discussed group tracking in [Blackman, 1986, chapter 11] and both subjects seem at first sight to be similar. Finally, it can be argued that the same equations V.1 to V.3 can be applied to clusters and yield the same properties. More research on this field must be pursued to finalize the formulation.

V.2.2 DataBase Management and Query Languages

In the proposed benchmark algorithm a data fusion database is included in the function. The information stored in this database is typical to a level 1 data fusion function where tracking and attribute data are stored [Waltz and Llinas, 1990, Chapter 10.2]. Waltz and Llinas have proposed some categorizations for their content of a typical level 1 database. For the data fusion function presented in Task IV where MHT data association and Track-While-Scan (TWS) mode is used, two important considerations must be taken into account. The access time for reading and updating must be quick since TWS allows a few mili second only, and the tracking data must include a hypotheses list and a cluster list.

Table V.2 below outlines the main information content which should be included for each object of a benchmark data fusion level 1 database. The MSDF database is a relational database made up of four tables or lists of objects. The maximum number of objects in each list is dependent on the limitations imposed on the MHT algorithm. For the proposed benchmark algorithm these limitations are indicated in figure IV.5 of Task IV.

As table V.2 shows, each track in the database is stored with a track number, the time of the last update and the positional data, state vector and covariance. The cluster index is the associated cluster number of the cluster list to which the track belongs. Track quality is a set of parameters which contains information about the status and state of the track (tentative, confirmed, number of misses, etc.) and the track priority is information related to the tactical importance of that track. The attribute information is a set of potential identities or target types. This information is stored using a pointer

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to the large threat database which is located in the identity estimation process. Each identity is saved with appropriate confidence value (support and plausibility if Dempster-Shafer is used). To facilitate the retrieval of information, the contacts which have been used to generate the track are indicated through the use of pointers attached to the contact list. Finally the hypotheses containing this track are also indicated by a pointer connected to the hypotheses list. The other objects are less information demanding and are also coupled by use of pointer data structure.

Table V.2. MSDF Database Information Content

Object	Typical Content	Approx. Size (byte) per object
Tracks	- Track number - Cluster index - Time of last measurement update - State Vector - Covariance matrix - Track quality - Priority index - Attribute data (identities) - Attribute confidence - Contact list (history) - Hypothesis list	200
Hypothesis	- Hypothesis number - Cluster index - Probability - Track list	50
Cluster	- Cluster number - Track list - Hypothesis list - Covered sector list	50
Contact	- Contact number - Time of the measurement - Reporting sensor - Measurement value - Variance value - Track list	50

The approximate computer memory size of the information to be stored is also indicated. The use of a pointer reduces the memory requirement. The total size of the complete database for the

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benchmark algorithms in Task IV can be estimated. Table IV.5 proposes a total of 256 tracks to be maintained. The number of contacts to be processed is 256 but in the database contacts saved for history there can be more. A maximum number of 2048 is probably sufficient. For the cluster there is no limit other than the number of tracks, but a number of 100 is certainly reasonable. For the number of hypothesis table IV.5 proposes eight per cluster. Therefore the total memory requirement of the MSDF database is around 200 Kbytes.

Concerning the query language of the MSDF database, existing general purpose relational database software is not recommended. The experience learned from CPF shows that a specifically tailored database with the appropriate query language optimized for the OMI monitoring purpose is preferable. The computer execution time is the main reason for such a requirement but the simplicity (due to its specific usage) of the database is also very beneficial. Its is not necessary to propose a sophisticated package such as ORACLE, INGRES, POSTGRES, etc.

V.2.3 Automated Fusion Processes as Decision Aids

In Task IV the suggested sensor data fusion function is used primarily for a surveillance system. It is designed to operate with a specific search and tracking process called track-while-scan. The set of benchmark algorithms perform a first level sensor fusion. The target model identification process discussed in Tasks I, II and III could include some fusion techniques to perform situation and target assessment. This last process has not been included in Task IV since a minimum set of algorithms was selected for the computer architecture evaluations.

For a strictly positional and attribute sensor fusion function, the rules of fusion are mathematical and do not require interpretation from operators. Consequently the fusion function was designed to work as an autonomous automatic sensor fusion function. The general information fusion (other than sensor fusion) is performed by the CCS operators, and the sensor fusion system acts as a decision aid in the accomplishment of the AAW frigate tasks. As mentioned, the proposed set of benchmark algorithms represent a minimum. Powerful computer processing of the future will permit the upgrade to include fusion processes to address the situation and target assessment. In this case not only sensor data will be fused but also any sources of information. Such fusion processes require Artificial Intelligence (AI) techniques not only in the processing of the information but also in the OMI. With intelligent OMI and an MSDF database using such object oriented and knowledge base rules as POSTGRES [Stonebraker, Hanson and Potamianos, 1988] the function would become a completely autonomous fusion function and at the same time, an efficient decision aids function [Waltz and Llinas, 1990, section 12.3.6].

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V.2.4 Recommendations Based on CPF Human Factors Studies

CPF has a distributed computer architecture. Within this architecture all operators could potentially have access to all the data available about the tactical situation and to all system functions. However, this could create confusion over the responsibility for actions and could flood the operator with too much information causing distraction. The CPF AN/UYQ-501 (V) Standard Display provides the capability for large and small Naval Tactical Display Symbols (NTDSs), colour, graphics (lines, circles, arcs), etc. On the CPF project many MMI analyses have been performed to evaluate which information is provided to which operator and how it is presented to them. Also the operational sequence of actions has been analyzed for different situations. Among these analyses the following have been of particular interest to the Canadian Naval Forces:

1. display layout
2. screen update rates
3. colour
4. operators access to functions
5. operator capability to filter information on the display
6. alarms and alerts
7. the usage of symbology and graphics on the display
8. MMI performance demonstration (sequence of actions in different scenarios), etc.

The details of these analyses are given below.

Display Layout: There are two display layouts required and specified within the CPF contract: one to display the tactical situation (TS); and the other to display hardware (HW) and software (SW) status information, called Page display. The TS display comprises the following areas:

1. Tactical Situation (TSA)

2. Auxiliary Readout (ARO) to display navigation and ship status information

3. Close Control Readout (CCRO) to display information about a selected target or contact

4. Data Amplification Readout (DARO) to display status or more detailed data about functions performed

5. Quick Action Buttons (QABs), a soft button grid, that can be selected to perform functions

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6. Operator Guidance Readout, an I/O area for the operator to enter textual data.

This is different from modern windowed environments. However each area was thoroughly analyzed in terms of what data was pertinent and what had to be suppressed to achieve efficient performance by the CCS operators. Hence this exercise provided a useful background into the type of data required to perform each function onboard a frigate type ship.

The Page display was designed to provide operators with the ability to evaluate and control the status of HW and SW while maintaining their ability to accept alarms concerning their functional responsibilities and to quickly return to their TS display. This display allows operator loading of specific SW configurations particular to tactical operating situations, and operator capability to perform online and offline maintenance of CCS subsystems without impacting the tactical operations.

These layouts also provide the operators with a common MMI for all their functions, thus reducing training time.

Screen Update Rates: The Navy officers were concerned about two issues when evaluating the screen update rates:

1. smooth track movement and accurate position of threats
2. flickering displays that could be distracting to the operators.

The track update rates were limited by the sensor and processing constraints, and an optimal update rate was selected. These update rates were made such that at small range scales fast targets (mach 3) travelled less than one symbol size between updates. All CCRO and DARO displays were designed in two components: permanent (template) and variable. Different colour was used for each. The variable components were analyzed to establish an update rate that minimized flickering and ensured timely, up-to-date information.

Colour: Many analyses were performed to establish the optimal use of colour within the constraints of the CPF Standard Display, the operator training considerations and tolerable system failure effects. To help select colour for CPF tactical displays which allowed the display of the NTDS symbols and graphics displays in all available colours, a prototype SW was developed. The following conclusions were derived:

1. Only a small number of colours can be usefully exploited. Different shades of the same colour should not be used. It is difficult to distinguish between shades which are not side-by-side, and it is difficult to ensure the same intensity, saturation and brightness on every display in the

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Operations Room.

2. For critical items, only mixed colours should be used (i.e., colours that are result of two or more colour guns, no red, blue or green) since if one of the colour guns fails, these items must still be visible.

3. Colour coding should be redundant with shapes, to ensure that colour blindness does not impact operation.

4. The colour red and blinking should be used in only extreme cases, to avoid distracting or inviting the operator.

Operator Access to Functions: The Navy Trades were studied to establish the CPF QAB array responsibilities. Then, many discussions were held with the Navy officers to finalize the functions (QAB arrays) available to each operator on the frigate. Each operator on CPF has a specific function e.g., Track Supervisor, Commanding Officer, Electronic Warfare (EW) operator, Radar Tracker, etc. The QAB arrays were analyzed to establish functions that are higher priority, that are accessed more often, or that must be accessible by every operator. For each operator, a hierarchical tree of QAB arrays are established where grouped functions have a logical relationship to facilitate learning and where more critical functions are located at the edges or corners of an array to make them more easily accessible. Common functions are provided in the same place on every array.

Information Filtering: In certain situations, when there are large numbers of targets and displays in the TSA, it can get so cluttered that the operators may have difficulty making decisions. The human engineering analyses in this case involved evaluating the information that could be optional to the operators. The operators were provided with QABs, which allowed them to filter the optional data in and out of the TSA. An example of such data are the local (not yet confirmed) EW or ASW contacts.

Alarms and Alerts: The analyses of alarms were again concentrated on which operators see which alarms, and what priority to assign to each one. Also an analysis of the colour of the alarms and alerts, and actions required to clear them was performed. The alarms are displayed in the bottom of the ARO and are red. The operators must sequence through the alarms to clear the alarm queue. A blinking "Alarm Pending" indicator notifies the operators about the alarms. More than one operator can receive an alarm. Some alarms require operators to perform a specific function (e.g., change the course of the frigate). In these cases, operators also receives an audible signal. Alerts are displayed in the ARO area in response to incorrect operator entries, and in the Page display at the top of the screen. They are the same colour as the templates on the pages (green), and they are displayed sequentially.

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The Usage of Symbology and Graphics: It was decided to use the small NTDS symbols in order not to clutter the TSA. Detailed analyses of graphics, such as radar sectors, search patterns, range rings, trial geometries, engageability displays, area of probability displays, bearing lines, etc. were performed to ensure that they do not clutter the TSA (to the extent possible), and they do not get misinterpreted as other displays, especially if the range scale is changed, or the Zoom function is used. Different line types are used (solid, dashed, etc.) for different objects, to discriminate between the complex aspects of a complicated display. If Zoom is likely to be used with a specific display, then solid lines are preferred to ensure their visibility after zooming.

MMI Performance Demonstration: For this analysis, scenarios were designed to simulate different situations and different threats that could be encountered by the frigate, then the sequence of operator actions required by design to cope with the situations were evaluated. These scenarios and corresponding actions were demonstrated and timed in the CSTSF. This analysis was used to evaluate whether the QAB array trees required any modification to optimize operator response, or if the operators required any additional capabilities to achieve their functions.

All these analyses have resulted in an automated CCS, where each operator has defined responsibilities, has access to all data required to perform his/her responsibilities, and his/her tools and decision-making processes are optimized to ensure best performance within the frame of the frigate's sensor and weapon capabilities.

V.2.4.1 The Impact of MSDF Implementation on CPF

The CPF AAW Sensor Allocation/Cueing Management (SM) function, Situation Assessment Decision Aid (SA) function, Emissions Warfare Resource Management (EM) function and Fire-Control Solution Derivation/Maintenance (FC) function, as well as the functions of trackers for every sensor system would be impacted by an implementation of an MSDF. The operators responsible for these functions would be required to have an understanding of statistical data analysis to be able to make intelligent conclusions about different solutions provided by MSDF, and to be able to perform the pertinent MSDF control actions. The MSDF should be perceived as a tracking function providing data of higher precision, which still needs operator intervention to distinguish between a number of possible interpretations of the target data, and whose performance could be improved by the actions of sensor trackers and operators supporting SM, SA, EM and FC functions.

Once the operators have the necessary background to understand the MSDF results, their MMI should not change significantly. Examples of changes to the display layout MMIs could be:

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1. A probability ellipse around the track symbology on TSA
2. An indication that a track is included in a number of alternate solutions
3. Information in the CCRO for each track about the confidence level of the selected solution
4. QABs to display the alternate solutions and to merge, confirm or delete solutions
5. QABs to derive solutions excluding the data from a specific sensor, or to localize MSDF analysis in a specific sector of interest.

These are just enhancements to the already available Track Management functions, and are consistent with CPF MMI philosophy.

The MSDF information and capabilities provided by the above MMIs will impact the performance of the operators in their usual functions in that they will know more about the targets they encounter, information more quickly available than with sensors alone. This is specifically important in the area of AAW where threats allow for very short reaction time. Hence incorporating MSDF processes will enhance the AAW performance of the CPF.

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ACRONYMS

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LIST OF ACRONYMS

AAM	Alignment Accelerometer Module
AAW	Anti-Air Warfare
ACDS	Advanced Combat Direction System
ACS	Afloat Correlation System
ADAM	Automated Data for Aerospace Maintenance
ADM	Advanced Development Model
ADT	Automatic Detection and Tracking
AFCEA	Armed Forces Communications and Electronics Association
AGARD	Advisory Group for Aeronautical Research and Development
AI	Artificial Intelligence
AMEP	Advanced Modular ESM Processor
ANN	Adaptive Neutral Network
AOC	Association of Old Crows
AOR	Operational Support Ship
AP	Associative Processor
AQAP	Allied Quality Assurance Publication
ARM	Anti-Radiation Measures
ARO	Auxiliary Readout
ASDC	Ada Software Development Centre
ASIC	Application Specific Integrated Circuits
ASSM	Anti-Surface Ship Missile
ASST	Anti-Ship Surveillance and Targeting
ASW	Anti-Submarine Warfare
ASWIS	ASW Information System
ATM	Alternative Tracks Method
ATR	Automatic Target Recognition
AUTOLIGN	AUTOmatic sensor aLIGNment
BAM	Bus Access Module
BBUS	BIU Interface
BF	Beam Frequency
BI	Serial Data Bus Interface (module)
BIF	Bearing Intercept Fix
BIU	Bus Interface Unit
BW	Beam Width
C^2	Command and Control
CAD	Computer-Aided Design
CAM	Computer-Aided Manufacturing

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LIST OF ACRONYMS

CPM	Conditional Probability Matrix
CANEWS	CANadian Electronic Warfare System
CASE	Computer-Aided Software Engineering
CB	Common Bus
CC	Cache Controller
CCP	Command and Control Processor
CCRO	Close Control Readout
CCS	Command and Control System
CE	CIO Environment Simulation (module)
CFAR	Constant False Alarm Rate
CG	Cruiser
CGN	Nuclear Powered Cruiser
CHP	[Chan, Hu and Plant]
CI	Loran-C Interface (module)
CIO	Communication Intercept Operations
CISTI	Canada Institute for Scientific and Technical Information
CIWS	Close-In Weapons System
CM	Cache Memory
CO	CIO Interface Simulation (module)
CoP	CoProcessor
COTS	Commercial Off-The-Shelf
CP	Central Processor
CPF	Canadian Patrol Frigate
CPU	Computer Processing Unit
CRAD	Chief Research And Development
CS	Combat System
CS	Common Routines (modules)
CSCI	Computer Software Configuration Item
CSCRS	Cost Schedule Control and Reporting System
CSTSF	Combat System and Test Support Facility
CV	Aircraft Carrier
CVBG	Battle Group Aircraft Carrier
CVN	Nuclear Powered Aircraft Carrier
DA	Data Association
DARO	Data Amplification Readout
DB	Data Base
DBMS	Data Base Management System

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LIST OF ACRONYMS

DD	Distributed Data Management (module)
DDG	Destroyer
DF	Direction Finding
DGMDO	Director General Maritime Doctrine and Operations
DH	Display Handler (module)
DM	Display Management (module)
DMCS	Directorate Maritime Combat System
DMCS-9	Director Maritime Combat Systems (Electronic Warfare)
DMCS-2	Directorate Maritime Combat System (Surface and Air)
DMCS-7	Directorate Maritime Combat System (Combat Systems)
DND	Department National Defence
DNR	Director Naval Requirements
DNR-3	Director Naval Requirements (Combat Systems)
DoD	Department of Defence
DP	Sim Display Support (module)
DPS	Data Processing Set
DR/DSMR	Dynamic System Monitoring and Reconfiguration (module)
DRAM	Dynamic RAM
DRE	Defence Research Establishment
DREA	Defence Research Establishment Atlantic
DREO	Defence Research Establishment Ottawa
DREV	Defence Research Establishment Valcartier
DS	CCS Display Support (module)
DSIS	Director Scientific Information Services
DSN	Distributed Sensor Network
DSS	Department of Supply and Services
DT	SPS-49 Radar Interface (module)
ECC	Eavedrops Cache Controller
ECM	Electronic CounterMeasures
EE	EW Environment Simulation (module)
EH	Error Handler (module)
EHI	European Helicopter Industry
EISG	Electronic Information System Group
ELINT	ELectronic INTelligence
EM	Electronic Warfare (EW) Management (module)
EM	Emission warfare resource Management
EMC	ElectroMagnetic Compatibility

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LIST OF ACRONYMS

EMCON	EMission CONtrol
EMI	Electro Magnetic Interference
EO	Electro Optic
EOT	Electro-Optic Tracker
EP	Enhanced Processor
ERP	Effective Radiated Power
ES	Expert System
ES	Electronic Support Measures (ESM) Interface (module)
ESM	Electronic Support Measures
EW	Electronic Warfare
EWS	Electronic Warfare Supervisor
EWSS	Electronic Warfare Simulation System
FC	Fire Control
FCS	Fire Control System
FFG	Frigate
FLIR	Forward - Looking Infra-Red
FM	File Management (module)
FPB	Fast Patrol Boat
FX	Fusion eXperimental
GDB	Global Data Base
GLSE	Generalized Linear least Squared Estimation
GP	Gyro Processing (module)
GR-UK	Greenland - United Kingdom
GST	Goods and Services Tax
HE	High Explosive
HEA	Horizontal Estimation Architecture
HF	High Frequency
HFE	Human Factors Engineering
hist	history
HVU	High Value Unit
HW	Hardware
I/O	Input/Output
IC	CIO Interface (module)
ID	Identification
ID	Identification (module)
IDS	Interface Design Specification
IEEE	Institute of Electronic and Electrical Engineers

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LIST OF ACRONYMS

IF	IFF Interface Simulation (module)
IFF	Identification Friend or Foe
ILS	Integrated Logistics Support
IMCS	Integrated Machinery Control System
IMM	Interacting Multiple Model
IMU	Internal Measurement Unit
INS	Inertial Navigation System
IOI	Input/Output Interfaces
IOP	Input/Output Processor
IOS	Information from Other Sources
IP	IFF System Interface (module)
IP	Instruction Processor
IPS	Interconnections Per Second
IPU	Information Processing Unit
IR	Infra-Red
IRAD	Internal Research And Development
IRST	Infra-Red Search Track
ISA	Industry Standard Architecture
ISI	Integrated Surveillance Integration
JDL-DFS	Joint Directors of Laboratories - Data Fusion Subpanel
JPDA	Joint Probabilistic Data Association
JPDAF	Joint Probabilistic Data Association and Fusion
JPO	Joint Program Office
KF	Kalman Filter
KBS	Knowledge-Based Systems
km	kilometre
kts	Knots (Nautical)
LAMS	Local Area Missile System
LOS	Line Of Sight
LPI	Low Possibility of Intercept
LRR	Long Range Radar
LTM	Long Term Memory
MA	Memory Array
MAP	Minimum A-posteriori Probability
MBP	Multidimensional Binary Partitions
MD	Multi-Sensor
MDE	Manoeuvre Detection and Estimation

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LIST OF ACRONYMS

MEWPADS	Maritime Electronic Warfare PAyload Development Study
MFR	Multiple(Multi-) Function Radar
MHT	Multiple Hypothesis Tracking
MHTC	Multiple Hypothesis Track Correlation
MI	Memory Interface
MIPS	Million Instructions Per Second
MLE	Maximum Likelihood Estimator
MMI	Man-Machine Interface
MMSE	Minimum Mean Square Error
MOE	Measure Of Effectiveness
MOP	Measures of Performance
MP	Maintenance Processor
MRR	Medium Range Radar
ms	millisecond
MS	Multi-Sensor
MSC	Modified Spherical Coordinate
MSDF	Multiple Sensor Data Fusion
MSDHS	Mission System Data Handling Subsystem
MSE	Mean Square Error
MSI	Multi-Sensor Integration
MSPDAF	Multisensor Probabilistic Data Association Filter
MST	Multi-Sensor Track
MTT	Multiple Target Tracking system
NA	Navigation (module)
NAAWS	NATO Anti-Air Warfare System
NATO	North Atlantic Treaty Organization
NB	Simulation Interface Unit Simulation (module)
NCCS(A)	Naval Command and Control - Afloat
NCNB	Non-Comment Non-Blank
NCTR	Non-Cooperative Target Recognition
ND	Inertial Navigation System (INS) Remote Display Interface (module)
NFR	NATO Frigate Replacement
NG	Inertial/Gyro/Navigator Interface Simulation (module)
NGS	Next Generation SHINPADS
NL	Loran-C Interface Simulation (module)
NLP	Natural Language Processing
nmi	nautical mile

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LIST OF ACRONYMS

NNSF	Nearest-Neighbour Standard Filter
NO	Omega Interface Simulation (module)
NS	Navigation Switchboard Interface (module)
NSA	New Shipborne Aircraft
NTDS	Naval Tactical Display Symbols
NUSC	Naval Underwater Systems Centre
OI	Omega Interface (module)
OMI	Operator-Machine Interface
OP	Operator Panel
OPEVAL	OPerational EVALuation
ops	Operations Per Second
PDA	Probabilistic Data Association
PDAF	Probabilistic Data Association Filter
PDF	Probability Density Functions
PE	Processing Element
PGC	Program Generation Centre
PGCC	Program Generation Control Centre
PH	Peripheral Handler (module)
PIPG	Paramax Information Products Group
PMV	Prime Mission Vehicle
PRF	Pulse Repetition Frequency
PRI/PW	Pulse Repetition Interval/Pulse Width
PTC	Propulsion Training Centre
PW	Pulse Width
QAB	Quick Action Button
QR	Quick Reaction
R&D	Research and Development
RA	SPS-49 ADT Interface Simulation (module)
RAM	Random Access Memory
RC	Radiation Control System Interface Simulation (module)
RCS	Radar Cross Section
RF	Radio Frequency
RFP	Request For Proposal
RFSS	Radar Frequency (RF) Signal Simulator
RMC	Royal Military College
RMF	Reconfigurable Modular Family
RMS	Root Mean Square

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LIST OF ACRONYMS

ROTP	Regular Officer Training Plan
RPV	Remote Piloted Vehicle
RS	SG-150 ADT Interface Simulation (module)
RWR	Radar Warning Receiver
SA	Situation Assessment
SC	Sim System Readiness/Control (module)
SCC	Simulation Control Centre
SDB	Serial Data Bus
SDI	Strategic Defence Initiative
SDX	Standard Distributed Executive (module)
SG	SG-150 Radar Interface (module)
SHINCOM	SHipboard INtegrated COMmunication
SHINMACS	SHipboard INtegrated Machinery Control System
SJSL	St-John Shipbuilding Limited
SL	System Loader (module)
SLCM	Submarine Launched Cruise Missile
SLOC	Source Line Of Code
SM	ESM System Interface Simulation (module)
SM	Sensor allocation/cueing Management
SMI	Serial Maintenance Interface
SN	Scenario Generation (module)
SNAF	Soviet Naval Air Force
SQL	Standard Query Language
SR	CCS System Readiness/Control (module)
SRP	Ship Replacement Program
SS	Conventional Submarine
SSAN	Auxiliary Nuclear Powered Submarine
SSBN	Nuclear Powered Balistic missile-armed Submarine
SSC	Services and Supplies Canada
SSGN	Nuclear Powered Guided missile-armed Submarine
SSKP	Single-Shot Kill Probability
SSN	Nuclear Powered Submarine
SSW	Surface-to-Surface Warfare
STM	Short Term Memory
SW	Software
TACTAS	TACtical Towed-Array Sonar
TDE	Target Data Extractor

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LIST OF ACRONYMS

TEWA	Threat Evaluation and Weapon Assignment
TG	Target Generator (module)
TM	Track Management (module)
TMA	Target Motion Analysis
TS	Tactical Situation
TSA	Tactical Situation Area
TTG	Time-To-Go
TWS	Track-While-Scan
UAV	Unmanned Airborne Vehicles
UCCS	Underwater Command and Control System
UD	Upper Diagonal
UDG	Unisys Defense Group
UDUT	Upper Diagonal Upper Transposed
UHF	Ultra High Frequency
URG	Underway Replenishment Group
USN	United States Navy
VA	minimum a-posteriori probability Viterbi Algorithm
VHF	Very High Frequency
VME	Virtual Memory Extended
VME	Versa Module Eurocard
WARM	WAr Reserved Mode
WBS	Work Breakdown Structure
WP	Warsaw Pact
WW II	World War II

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Investigation on Target Tracking and Classification Using Multiple Sensor Data Fusion

Task IV - Evaluation of Hardware / Software Processing Architecture

Task V - Study of Displays and Man-Machine Interface

Technical Report

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